Electronic Supplementary Information

A facile route to the fabrication of large-scale gate-all-around nanofluidic field-effect transistor with low leakage current

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1. TEM samples prepared by the FIB technique

The TEM samples were prepared by the FIB technique. Prior to cutting the cross-section of the nanofluidic FET structure, a thin organic layer followed by a platinum layer were deposited in order to protect and reinforce the thin TEM samples from the gallium ion beam.

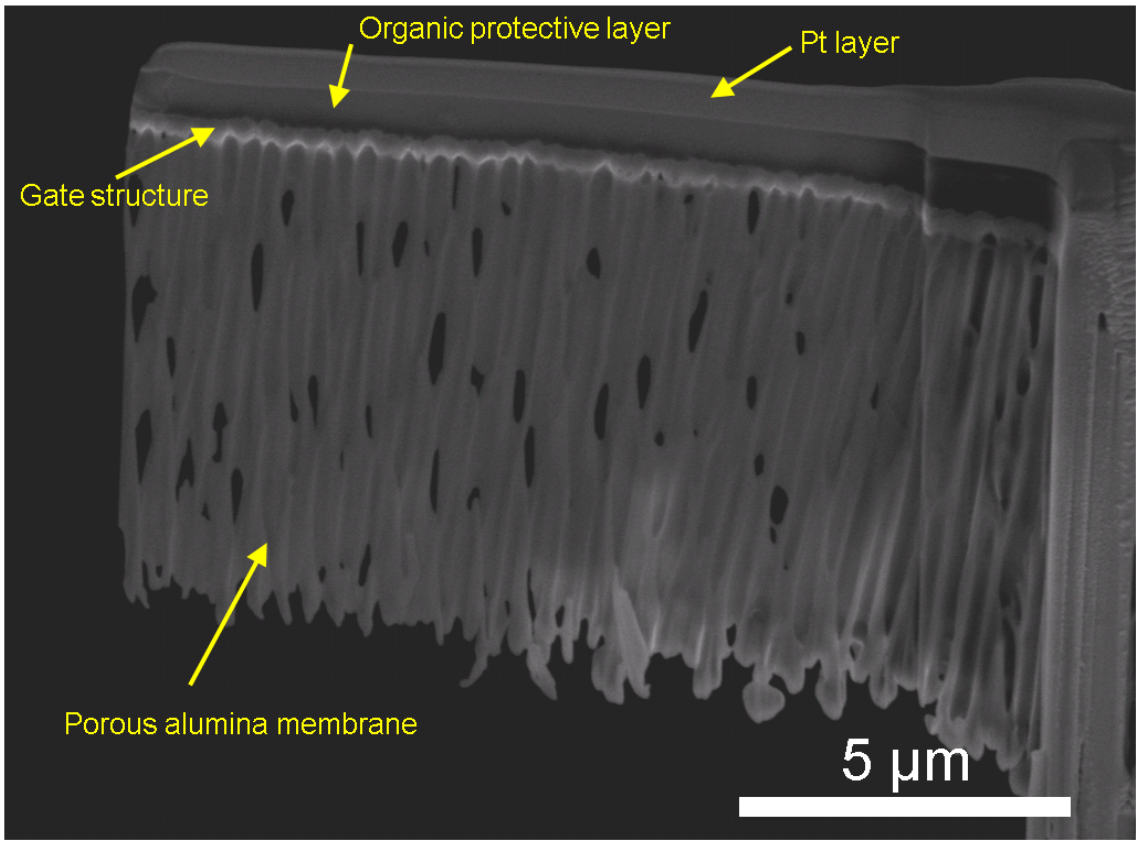

Figure S1. SEM image of the TEM sample prepared by the FIB technique.

2. Experimental setup

A schematic of the experimental setup for gate leakage and gating experiments is presented in Figure S2. Between the two electrolyte reservoirs, a gate-attached AAO membrane was inserted. The AAO membrane was attached to a slide glass with the gate structure facing upwards. An access hole was drilled on the slide glass. A silicone rubber gasket was placed between the glass slide and the reservoir to completely seal the device. Black lines depict circuit configurations for the gating experiments (for Figure 6) whereas red lines represent configurations for the gate leakage experiments (for Figure 4). All current measurements were conducted inside Faraday cage.

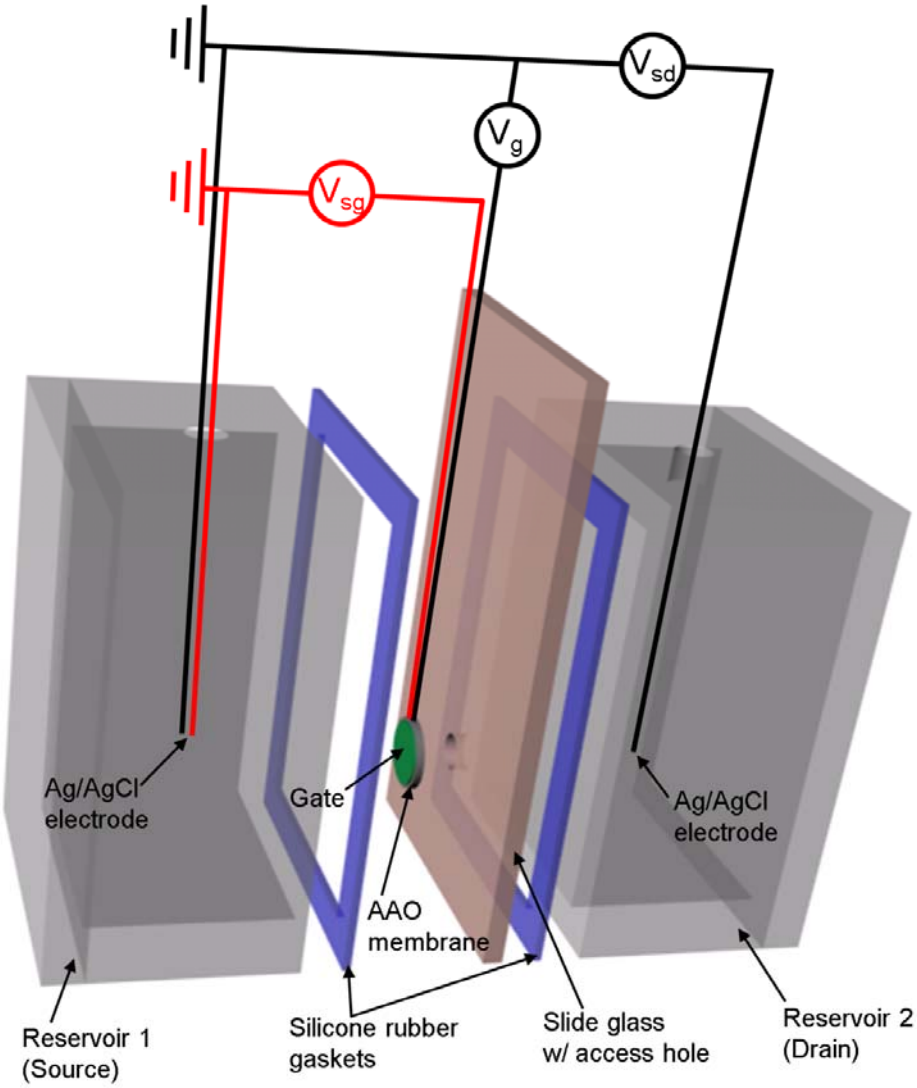

Figure S2. Schematic of the experimental setup used for the gate leakage and gating experiments. Black lines depict circuit configurations for the gating experiments whereas red lines represent configurations for the gate leakage experiments.

3. EDS results on the aluminum-alumina structure

Point elemental analysis was done for the two different samples. Figure S3 (a) and (b) both confirms the existence of oxygen in the edge of aluminum layer, which implies the formation of an alumina layer.

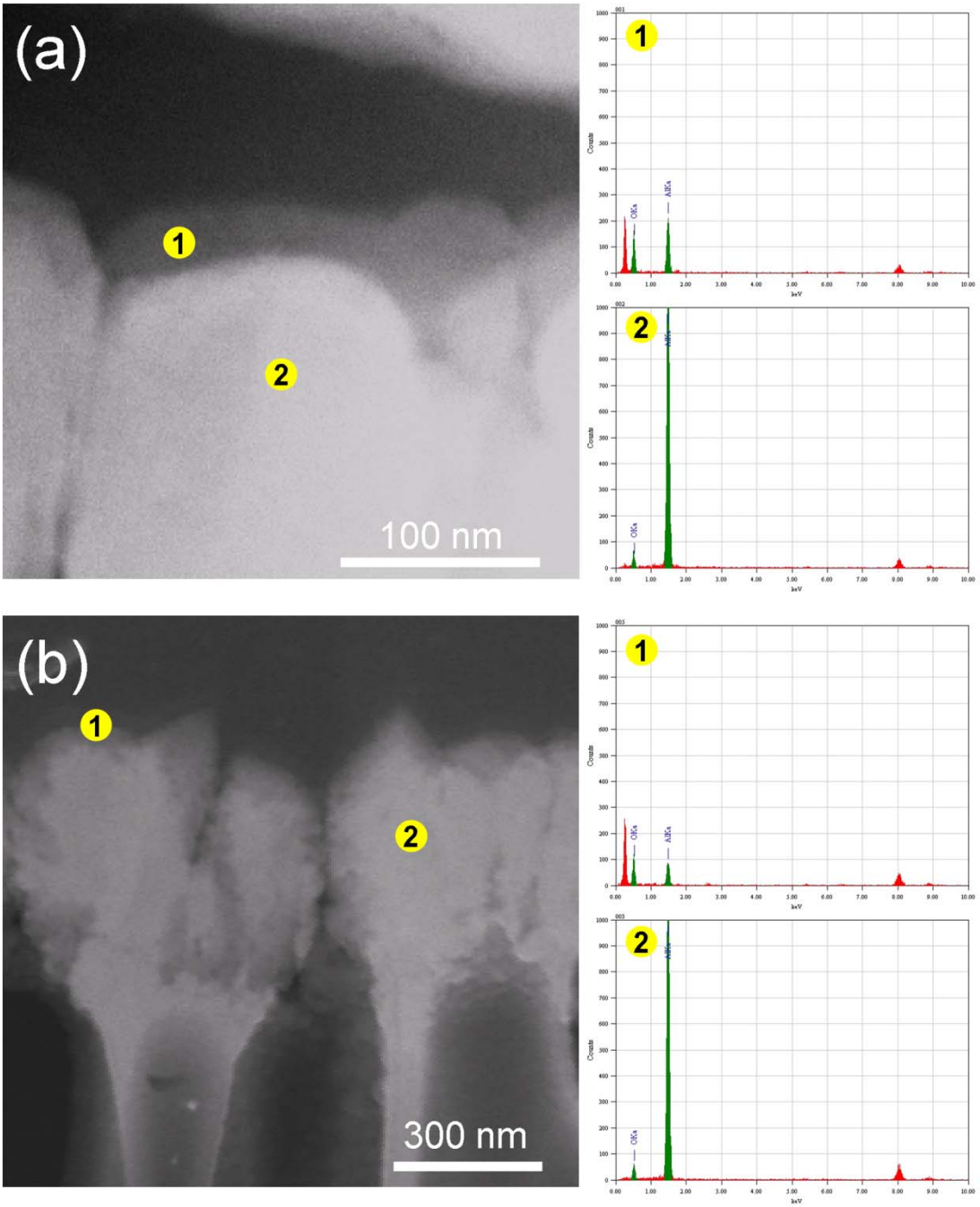

Figure S4. Scanning TEM images of the nanofluidic FET structures for V_a of (a) 10 V and (b) 6.15 V and its corresponding point EDS results. Mark 1 denotes the area in the alumina whereas mark 2 denotes area in the aluminum.

4. Estimation of nanochannel size due to volume expansion during anodization

As the anodization proceeds, the volume expands approximately doubles the original volume because the atomic density of aluminum in alumina is about half than in metallic aluminum (J. Choi, *Fabrication of Monodomain Porous Alumina using Nanoimprint Lithography and its Applications*, PhD Thesis, University of Halle-Wittenberg, **2004**). Because the length increases with a cube root of volume increase, the thickness of the alumina is increased by 26% to its original value; this corresponds to an additional thickness increase of 5.2 nm for a 20 nm-thick alumina layer (V_a = 10 V) and 3.9 nm for a 15 nm-thick alumina layer (V_a = 6.15 V). Therefore, the pore will be narrowed by 10.4 nm and 7.8 nm, which leads to a final pore size of 17.5 nm and 20.1 nm for V_a of 10 and 6.15 V, respectively.

5. SEM images of gate dielectric layers formed by other methods

The primary goal of this study was to realize a robust, leak-free gate dielectric for the gate-all-around nanofluidic FET with minimum effort and cost. Prior to choosing anodization as a method to form the gate dielectric layer, we tried various sorts of other deposition methods. At first, conventional gas-phase deposition methods were tried: PECVD for silica, sputter for alumina, polymer coating in Bosch process (deep reactive ion etching) for CF_4, and parylene coater for parylene-C. However, none for these methods were satisfactory despite the good step coverage. The deposited dielectric layer seemed to be irregularly formed or even partially agglomerated (Figure S4). The surface of the Anodisc® was too rough to be completely covered by such gas-phase methods. Therefore, we moved on to solution-phase methods in order to form the dielectric layer under the most similar condition to the nanofluidics experiments. Non-conducting self-assembled monolayers (SAM) of various chain lengths of *n*-alkanethiols ($CH_3(CH_2)_nSH$) were first tested. Propane- (*n*=2), dodecane- (*n*=11), hexadecane- (*n*=15) and octadecanethiol (*n*=17) SAMs were formed on the gold surface. However, they were also failed to insulate the gate metal because of the extreme surface roughness (J. C. Love, L. A. Estroff, J. K. Kriebel, R. G. Nuzzo and G. M. Whitesides, *Chem. Rev.*, 2005, **105**, 1103-1169). Low van der Waals interactions for short-chained SAMs and incomplete packing at concave surfaces for long-chained SAMs may have resulted in numerous pin-holes that should lead to poor insulation quality (F.-M. Boldt, N. Baltes, K. Borgwarth and J. Heinze, *Surf. Sci.*, 2005, **597**, 51-64).

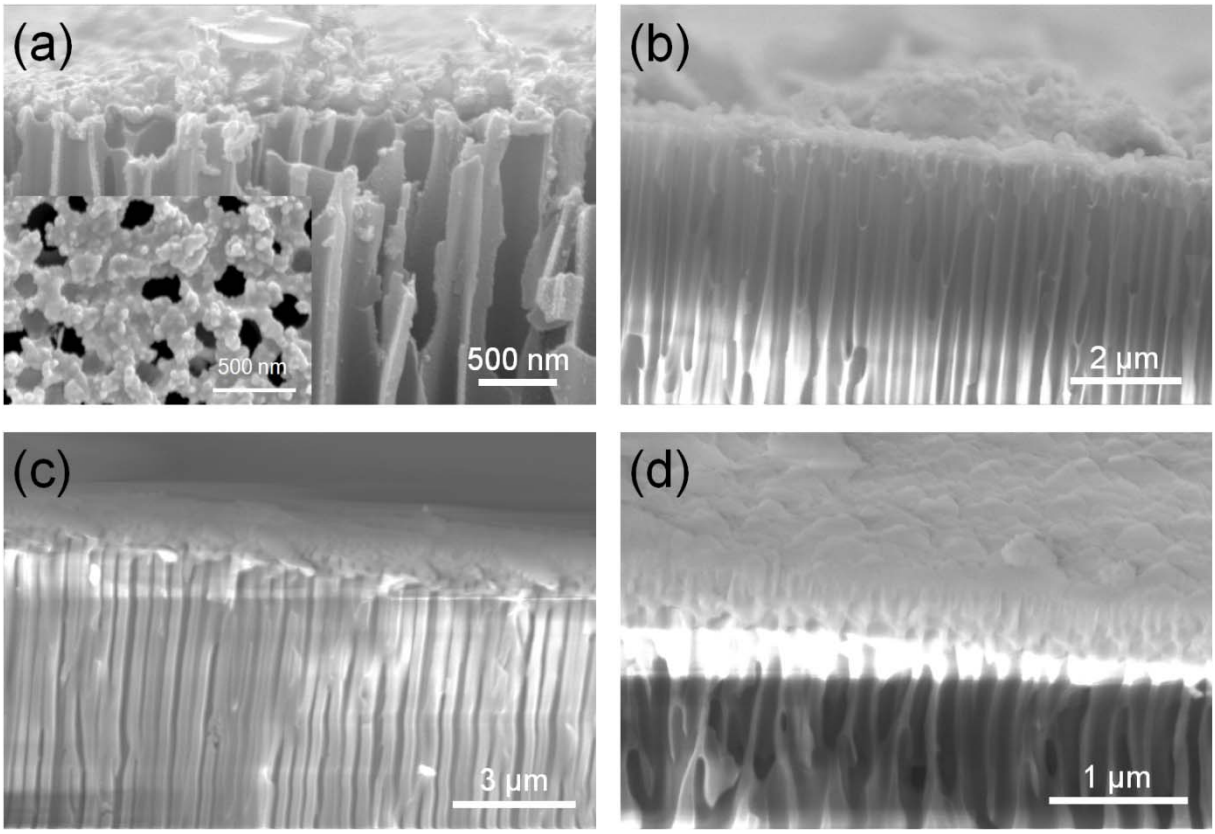

Figure S4. SEM images of the cross-sections of Anodisc® covered with (a) CF_4 by polymer coating in Bosch process, (b) parylene by parylene coater, (c) alumina by sputtering, and (d) silica by PECVD on a gold coated surface. Inset in (a) shows top view of the CF_4-coated surface which clearly shows non-uniform pores due to the particle-like agglomeration.

6. Comparison of technical features of various nanofluidic FETs

Table S1. Technical features of various nanofluidic FETs from the references.

Reference	Channel type	Channel size [nm]	Gate type	Gate dielectric thickness [nm]	Gate dielectric formation method	Gate voltage range [V]	Onset of gate leakage [V]	
							Negative gate voltage	Positive gate voltage
[11]	Microfabricated channel	35	Planar	600	LPCVD [a]	-75~75	N/A	N/A
[11]	Silica nanotube	10~100	Fin	30~40 [b]	-	-20~20	N/A	N/A
[12]	Mesoporous silica (SBA-15)	4~5	Planar	3~4 [c]	-	-1~1	-0.5	-
[13]	Nanopatterned hole array	1	All-around	35~40	ALD	-1~1	-3	1
[14]	Track-etched single conical pore	5~15	All-around	50	E-beam evaporation	-0.8~2	-	-
[15]	Nanopatterned single pore	20	All-around	25	ALD	-0.5~0.5	-	-
[16]	Nanopatterned hole array	34, 95	All-around	60	Thermal oxidation	-10~10	-1	-
This work	Anodisc® pore array	20.1, 17.5	All-around	15, 20	Barrier-type anodization	-2~2	-3	3

[a] Low-pressure chemical vapor deposition
[b] Silica nanotube wall thickness
[c] Mesoporous silica wall thickness