Electronic Supplementary Material (ESI) for Lab on a Chip

Supplementary Information

Flow modeling-based trap design

One of the most basic trap designs for sieve-like traps for cell trapping has been described and reported by Di Carlo et al[1]. The design is a cup-shaped trap for the capture of an isolated single cell. A distinct feature in Di Carlo's trap for reducing multiple cell trapping is to introduce a gap between the substrate and the traps for fluidic resistance to be altered according to the occupancy of the traps. For the purpose of our flow modeling, a gap of 5 μm was used. Besides making use of changes in fluidic resistance, we believe that the shape of the traps also assisted in reducing multiple cell trapping. Compared to the broad, flat sides in Di Carlo's design, sharp, pointed sides of the traps would possibly allow incoming cells or multiply trapped cells to slip off occupied traps, particularly if a flushing step is performed after cell trapping.

To maximize streamline flow into the traps, we commenced with a modified version of Di Carlo's basic trap design and gradually "opening up" the trap (see Fig. S1). The maximum size of the opening was maintained at 5 μm to prevent cells from being able to "squeeze through" them. By a flow of simulated particles (particle density = 6.67 particles/μm) through different trap designs, the trapping efficiency of each trap was characterized by counting the number of simulated particle tracks that passed through the trap. The trap design that allowed more simulated particle tracks to pass through was likely to have a higher trapping efficiency under experimental conditions. Most of the simulated particles were diverted away from the traps, as expected due to the high fluidic resistance around it. The optimized design for cell trapping was determined as a three-block configuration, with an increase from 6 to 30 simulated particle tracks passing through the trap as compared with a "closed up" design. The particle tracks were overlaid with velocity magnitude contours to give an indication of the fluidic resistance around the traps. In the optimized three-block design, the region of low velocity magnitude (See Fig. S1, dark blue colour map) or high fluidic resistance in the trapping region is the smallest, possibly due to the openings in the trap that allows streamlines to flow through. Hence, fewer particles were observed to be diverted away from the trap. Such openings in the trap also complemented the single cell trapping mechanism mentioned.

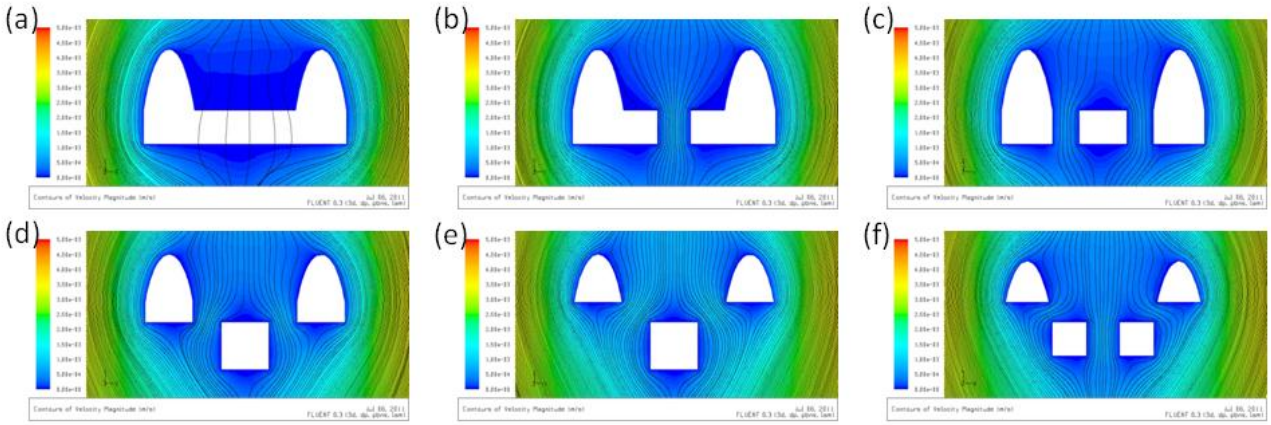

Fig. S1 Particle tracks (black lines) of simulated particles overlaid with velocity magnitude contours (red: highest, blue: lowest). Different trap designs were characterized by counting the number of particles flowing through the trap. (a) No openings, 6 particle tracks through trap. (b) 1 opening, 14 particle tracks. (c) 2 openings, 12 particle tracks. (d) No corners, 20 particle tracks. (e) No corners with side openings, 30 particle tracks. f) 4-piece configuration, 20 particle tracks.

Microchannel fabrication

The gap distance between the sieve-like traps and the bottom cover slip substrate is a critical feature in the cell-positioning platform. Besides enabling single cell trapping and to vary the fluidic resistance according to the occupancy of the traps, this gap also protects the fibronectin layer by preventing contact between the trap and the pattern. Furthermore, it enables trapped cells to spread partially underneath the trap on the protein pattern to facilitate stronger cell attachment to the substrate before removal of the microchannel. From a fabrication standpoint, to achieve such a gap between the trap and the glass substrate, the trap and the microchannel wall needed to have different heights, such that the traps were slightly shorter and avoided contact with the fibronectin-patterned substrate.

Usually, to fabricate surface features of different heights, an additional fabrication step is involved for each feature height with an alignment step in between. Such a multi-step process increases the complexity of fabrication, and may yield defects related to misalignment of features or inaccurate control of the fabricated depth in each step. Here, we describe a straightforward one-step method to fabricate features of different heights, taking advantage of the reactive ion etching lag (RIE-lag) present in the silicon Bosch dry etch process. When etched to a significant depth using this process, the etch rate of higher aspect ratio features has been shown to be slower than those with lower aspect ratios, an effect termed 'RIE-lag'. In our microchannel, the traps and side pillars have a much smaller aspect ratio as compared with the channel walls. When etching all these features in one step, the traps and side pillars will be etched slower than the channel wall, creating the different feature heights (see Fig. S2a). This difference in feature heights will translate into the required gap between the traps and the micropatterns when the microchannel is bonded to its substrate. The degree of RIE-lag can be influenced by the etching time as reported in a 3-stage model (deposition, polymer removal and etching) used to account for RIE-lag effects[2]. We have shown that by varying the etching time in our protocol, the difference in etch rate between the trap and the channel walls can be controlled. This translates to some control of the gap size between the trap and the substrate (see Fig. S2b).

After the fabrication of the master, the microchannel device is replicated using PDMS soft-lithography. Heat curing of PDMS has been reported to induce shrinkage in the PDMS features depending on the curing conditions[3]. This phenomenon leads to size deviations from the mold dimensions of the PDMS structures and as result causes a mismatch between the positions of the sieve-like traps and that of the protein micropatterns. The management of this mismatch is of very high importance as it plays a crucial role in determining the overall throughput of the cell positioning platform. The degree of PDMS shrinkage has been shown to be dependent on the curing temperature and when cured at room temperature for 72 hours, the PDMS shrinkage is negligible. However, we have observed that the PDMS devices that were cured at room temperature caused cell bebbling, an indication of cytotoxicity. Therefore, we suggest that room temperature curing only results in partial curing of the PDMS even over long period of curing time. Diffusion of non-crosslinked PDMS pre-polymer into the small volumes of fluid in the microfludic channel could possibly create an environment unsuitable for cell survival[4]. To lessen this problem, we devised a two-step curing process where PDMS is first cured at room temperature for 72 hours followed by heat curing at 60 °C for 5 hours for a more complete curing of the PDMS. Using this process, cell bebbling effects are eliminated and PDMS shrinkage ratio is significantly reduced (data not shown). Alternatively, we proposed a 1% offset in the photolithographic mask design for the microchannel and to fine tune any size deviations from the patterned substrate with curing temperature.

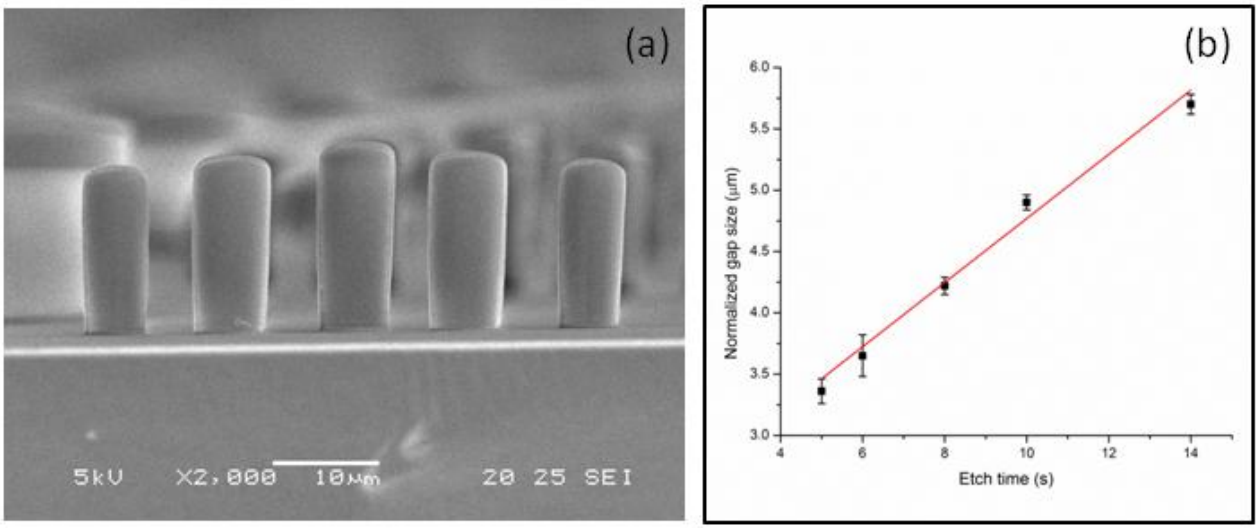

Fig. S2 Characterization of gap size differences in the microchannel at different etch times used in deep silicon etching. (a) Cross-section SEM image used to measure the feature height. This example show features etched at 8-sec etching time per cycle of the Bosch process. (b) Normalized gap size as a function of etching time per cycle used in the process recipe. Gap sizes were measured from the 2nd and 4th pillar from left in (a). The gap size is normalized to approximately what it would be if the channel walls were etched exactly to 20 µm.

Supplementary References

1. D. Di Carlo, N. Aghdam and L.P. Lee, *Anal. Chem.*, 2006, **78**, 4925-4930
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4. K.L. Regehr, M. Domenech M., J.T. Koepsel, K.C. Carver, S.J. Ellison-Zelsko, W.L. Murphy, L.A., E.T. Alarid and D.J. Beebe, *Lab Chip*, 2009, **9**, 2132-2139