Electronic Supplementary Material (ESI) for Lab on a Chip

Supplementary Material

An Intelligent Digital Microfluidic System with Fuzzy-Enhanced Feedback for Multi-Droplet Manipulation

Jie Gao[a,#], Xianming Liu[b,#], Tianlan Chen[a], Pui-In Mak[a], Yuguang Du[b], Mang-I Vai[a], Bingcheng Lin[b*] and Rui P. Martins[a, c*]

[a] State-Key Laboratory of Analog and Mixed-Signal VLSI,
University of Macau, Avenida Padre Tomás Pereira, Taipa, Macao, China

[b] The Research Centre of Lab on a Chip, Dalian Institute of Chemical Physics,
Chinese Academy of Sciences, Dalian, 457 Zhongshan Road, Dalian, China (116023)

[c] on leave from Instituto Superior Técnico, Technical University of Lisbon, Portugal

[#] Authors who made equal contributions.

ESI Text

DMF Chip Fabrication and Assembly. The fabrication procedure is shown in Fig. S1.

Step 1-2: The electrodes of the bottom plate were drawn in AutoCAD (Autodesk, Inc.) and patterned on Cr-coated glass with standard lithographical and wet-etch methods.

Step 3: The Ta_2O_5 dielectric layer was deposited by reactive DC magnetron sputtering (HHV, Auto 500) at room temperature with a 99.99% Ta target under an Ar/O_2 ambient. The chamber was pumped down to 1.3×10^{-4} Pa and backfilled with the sputtering gas with 15 sccm Ar and 2.05 sccm O_2. The power was set at 110 W, producing a deposition rate of 2.4 nm/min. Different thicknesses of 180 nm, 115 nm and 65 nm Ta_2O_5 layers were obtained by regulating sputtering time. The oxidized layer was rapid thermal annealed in a N_2 atmosphere (20 sccm) at 400 °C for 10 min to reduce the number of pin-holes in the dielectric.

Step 4: The surface of the chip was primed by silane solution (Silquest A-174 Silane, Momentive Performance Materials) in isopropyl alcohol for 15 min to enhance adhesion between Ta_2O_5 and Parylene C coatings. It was then baked at 120 °C for 5 min.

Step 5: Low pressure chemical vapor deposition method (La-Chi, LH300) was adopted to deposit Parylene-C layer (360 nm) on top of Ta_2O_5 surface. This extra layer covered the pinholes in Ta_2O_5 layer and prevented their exposure to liquid samples. In the meantime, a portion of the high dielectric constant and strength of the Ta_2O_5 were maintained (1).

Step 6-8: Amorphous fluoropolymer hydrophobic layers of 100 nm thickness was obtained by spin coating 0.5% Teflon® AF (1601S, Dupont) in perfluorosilane (FC-40, 3M) at 3200 rotation per minute (rpm) for 60 s on the bottom plate and the top plate, which was made of Indium Tin Oxide-coated glass, followed by being treated at 160 °C for 4 hours.

Step 9: A space of approximately 200 μm was made by metal tapes between the top and the bottom plate with their hydrophobic layers facing each other. Silicone oils (polydimethylsiloxanes) were used as transport media due to their low surface tension and the availability of low viscosities (1 cSt, Clearco). Droplets were applied with a pipette (Rainin, Mettler Toledo) unless otherwise indicated.

Chip Holder. The main body (Fig. S2, top layer) is made by PMMA (Acrylic) and is ergonomically sized as 20 x 20 x 2.5 cm (L x W X H) to be fitted for the human operator.

The DMF chip is mounted with two 12-pin IC Test Clips (3M) for droplet sensing and voltage actuation. Front and back sides of the main body are left blank for easy test-clip on/off to replace the DMF chip. On top of the DMF chip there is an ITO glass featuring high electrical conductivity on the bottom side. The edges of the ITO glass are twined by conductive tape. Conductive tape at the bottom of the ITO glass serves as the spacer leaving space for droplet movements. Tuning or increasing the layer of the conductive tape can adjust the height of the spacer. Conductive tape at the top of the ITO glass is fixed by glass clips. The bottom side of the ITO glass is connected to the glass clip that is electrically grounded.

Control Electronics. The printed circuit board (PCB) (Fig. S2, mid layer) was drawn with Altium Designer with a dimension of 20 x 20 x 1.5 mm (L x W X H). The control electronics is to interface the DMF chip with the field-programmable gate array (FPGA). There are 25 electrically-controlled relays (Fig. S3) mounted on the PCB for connecting the DMF chip with the driving voltage or the oscillator. To allow a wide driving-voltage range from 0 to 80 V AC, a low-cost relay (HRS2H-S-DC5V HKE®) is selected. It features a life cycle of 100,000 times, impact resistance voltage 1500V AC, pickup and release times of maximally 7 and 3 ms, respectively. The current withstand limit is up to 1 A at 120 V AC. To support a total of 24 electrodes frequency measurement for the DMF chip, two high-speed Si-gate CMOS 16-channel analog multiplexers (74HC4067 NXP Semiconductors) were employed. Its rise and fall times are 500 ns at 4.5 V. The relays and multiplexers are controlled by the FPGA. The driving voltage is a 1 kHz square wave supported by a low-cost signal generator (GFG-8255A Instek®).

The first signal relay is initially grounded to avoid command error, letting the driving signal to be connected to the DMF chip. The remaining 24 signal relays are switched to the multiplexers initially. When the system is idle, the FPGA can keep sweeping all 24 electrodes to measure the responding frequency (respond to the change of capacitance) by multiplexing each electrode to the oscillator. To manipulate the droplets, the destination electrode should be connected to the driving voltage while the oscillator circuit is separated to the DMF Chip.

Field-Programmable Gate Array (FPGA) Board. The hardware control (Fig. S2, bottom layer) is implemented by a FPGA board (Altera Cyclone® II 2C70 device). The hardware language is Verilog. The internal units include data transfer, frequency detection, data collection and operation controller. The clock rate is 50 MHz. When the system is idle, the FPGA will keep sweeping all 24 electrodes on the DMF chip (Fig. S4). Each is sequentially multiplexed to the oscillator, and stands for 0.5 ms to escape the transient and then measure the frequency. The responded frequency is roughly 100 kHz while the frequency counter is clocked at 50 MHz and therefore a MHz-range measurement precision is achieved. After sweeping the 24 electrodes, the FPGA sends the 24 counting values to the computer for further processing via a serial port with a speed of 115,200 bit/s. The computer based on the capacitance value of each electrode evaluates the presence/absence of a droplet, and then maps it to a 4 x 6 matrix as in the DMF chip. The control command transferred from computer software via the serial port includes the location of the droplet and the time duration of the charging. When the operation of the FPGA is complete and there is no command received, the system returns to idle mode, and sweeps again all electrodes to scan their capacitances.

Software-Defined Operation Unit. The software engine is compiled by Microsoft® Visual Studio® 2010 in C#. When the DMF module is ready, the operation unit collects the capacitance values of each electrode from the FPGA (Fig. S5). By comparing with their initial values (i.e., no droplet), the software can preliminarily detect the droplet location. Even if the droplets are drifting, the software can still track the position of the droplets after positioning calculation, to fine-tune the droplet position. Fuzzy control theory is applied to facilitate the computer to generate the charging time which must be applied to the target electrode. By setting up an expert knowledge database with the experienced DMF operator, the fuzzy controller built in MATLAB® can operate according to the position between the target electrode and its adjacent to optimize the charging time. When all droplets are precisely positioned, the software engine can be programmed to execute a number of complex operations befitting different chemical or biological experiments. During the proceedings, the system will check the knowledge, pre-set rules and droplets location to generate each droplet routing on the chip with less movement, in order to extend the life time of the chip and avoid the unnecessary merging.

1 Y. Y. Lin, R. D. Evans, E. Welch, B. N. Hsu, A. C. Madison and R.B. Fair, *Sens Actuators B Chem*. 2010, **150**, 465-470.

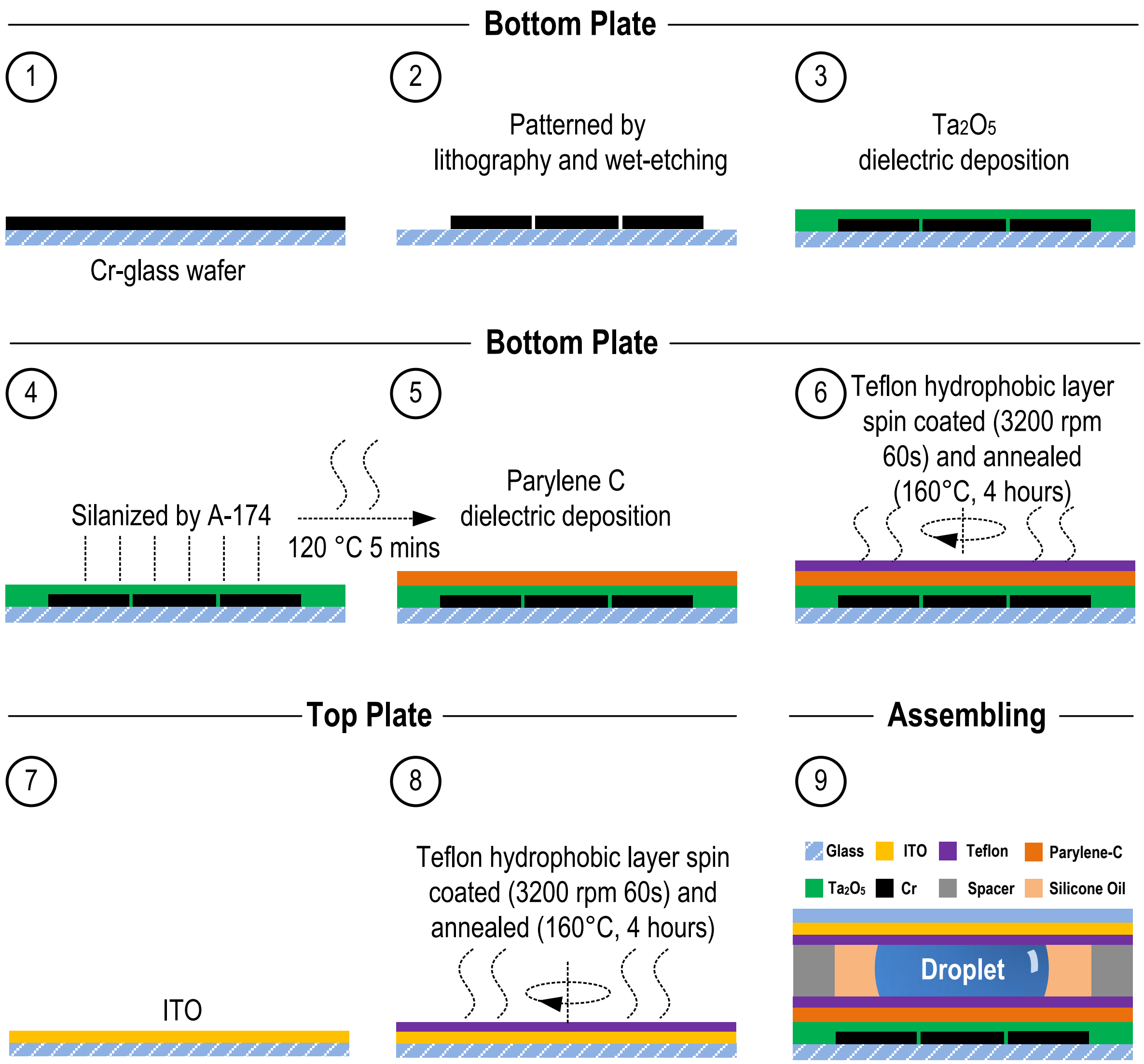

Fig. S1. Fabrication procedure of Ta_2O_5/Parylene C-insulated two-plate DMF chip. The fabrication of the bottom plate (steps 1 to 6), was conducted on a Cr glass with standard lithography and wet etching. Ta_2O_5 and Parylene C were deposited on top of electrodes as dielectric layers with spun-on Teflon offering hydrophobicity; the top plate (steps 7 and 8) was made from ITO glass after it was treated with Teflon. Separated by a spacer, droplets and oils were applied on the bottom plate. The two plates were placed facing each other and assembled to complete the DMF chip (step 9).

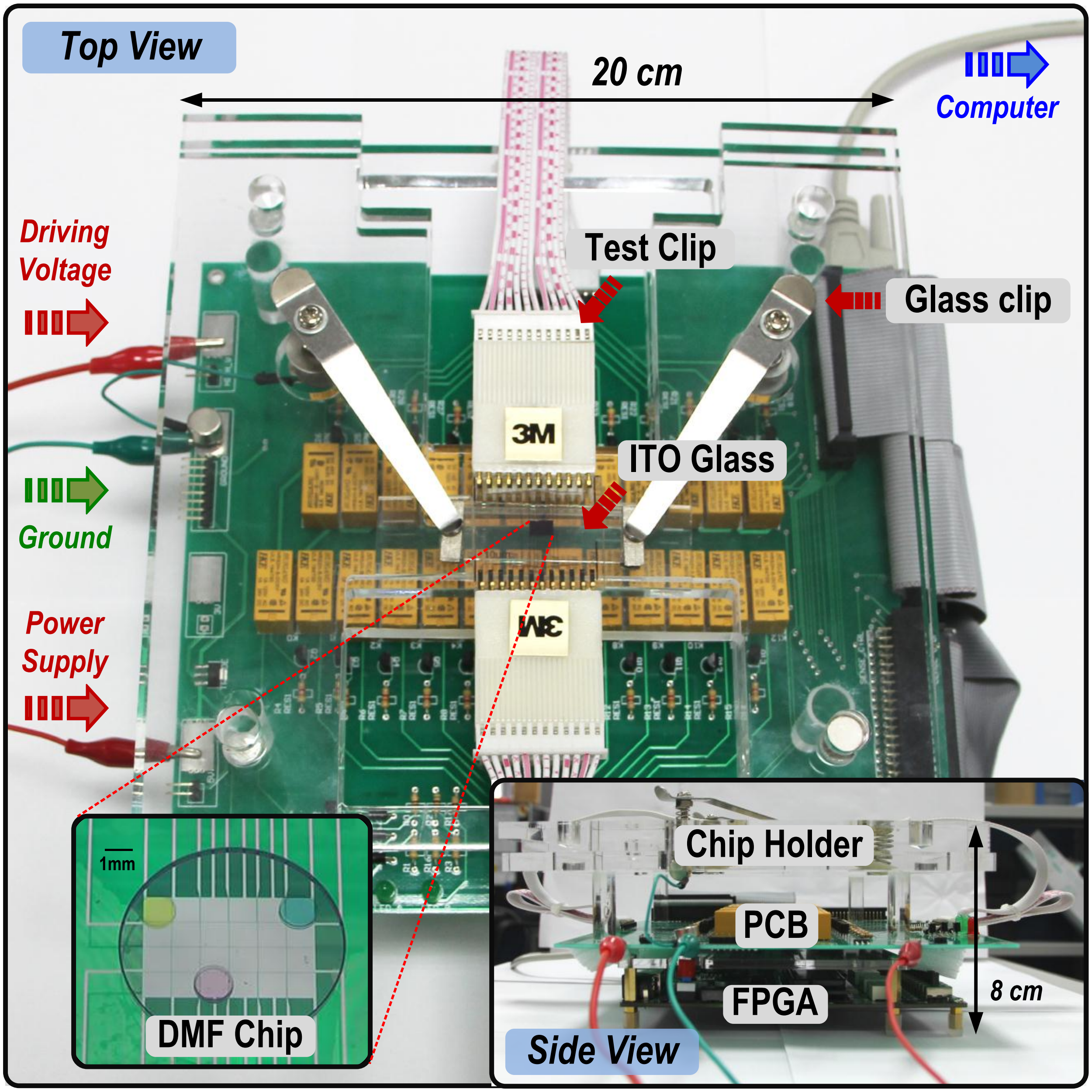

Fig. S2. The hardware of the intelligent DMF system includes three operation layers: DMF chip holder (top layer), control electronics board (mid layer) and field-programmable gate array (FPGA) board (bottom layer). The DMF chip holder is to mount the DMF chip. The control electronics on the printed circuit board (PCB) is to apply driving voltages (acquire capacitance information) to (from) the DMF chip. The FPGA acquires the signal from the control electronics and transfers it to the computer. The entire module is sized to fit human hands for easy mounting the DMF chip and ITO glass with chip and glass clips. The IC test clips connects the DMF chip to the control electronics. The relay array and multiplexers switch the DMF chip between the driving voltages (actuation) and oscillator (sensing).

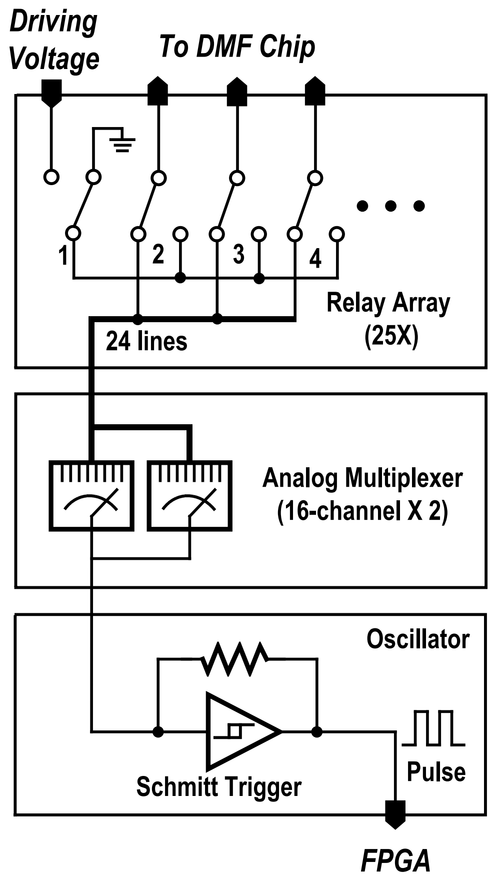

Fig. S3. There are 25 relays within the control electronics with the first separated from the remaining 24 which are connected to the DMF chip. The first relay will be switched to the driving voltage when the DMF chip is to be accessed. Initially two analog multiplexers are directly connected to the 24 relays while there is only one channel opened for frequency measurement via an oscillator. The oscillator is built by a Schmitt Trigger and resistors which will generate different frequencies with respect to the sensed capacitances.

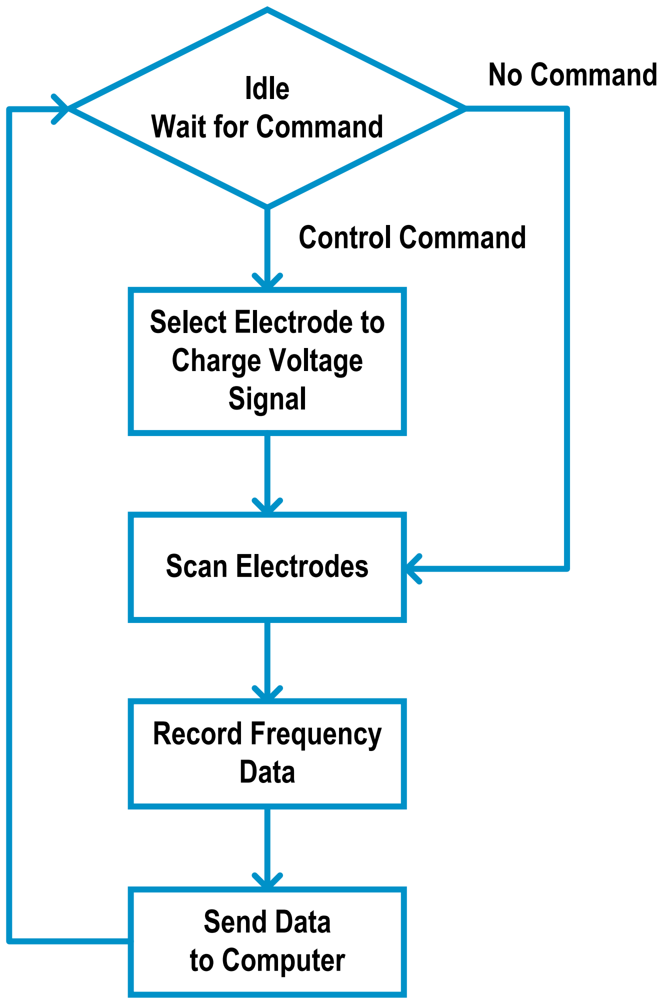

Fig. S4. The FPGA controller in the idle state will wait for the control commands. When no command is received, the FPGA controller will scan the electrodes in order to measure their responding frequencies. The frequency data are recorded and sent to the computer. If there is a control command received, the driving voltage will charge the target electrode before scanning the electrodes and other steps.

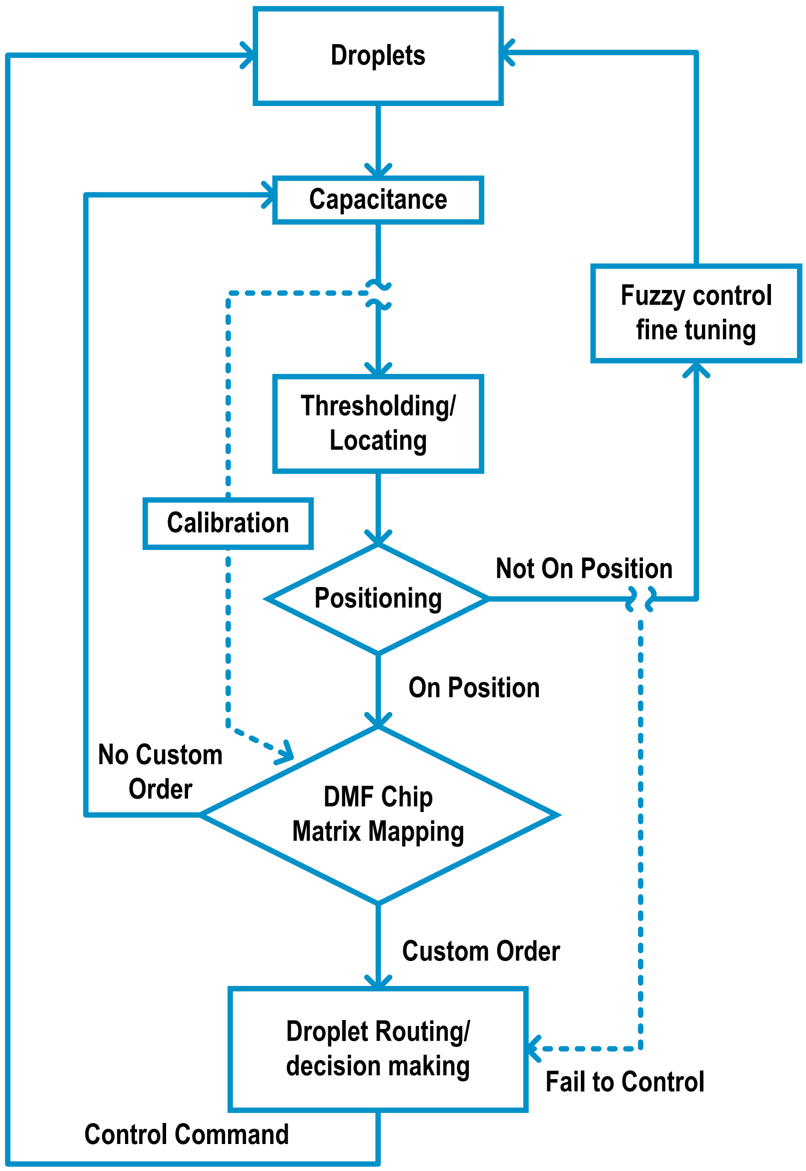

Fig. S5. The DMF system features self-calibration ability to initialize the capacitance value and record the threshold value of each individual electrode. For the DMF chip matrix mapping, capacitance of electrodes will be compared to the threshold value. A more precise droplet positioning is to be fine-tuned with the fuzzy-enhanced software engine. Custom order can be a pre-set sequence or an instant command inputted by the operator. Before sending out the control command, the system will check the knowledge base, pre-set rules and droplets location for droplet movement in order to achieve an optimum routing. If a specific route is not successful (e.g., involve a deteriorated electrode), the system will try another alternative to complete the custom order.

Electronic Supplementary Material (ESI) for Lab on a Chip

Table 1 Fuzzy Rule Base

Membership function				
Input1	Input2	Output		
Position	Voltage	Gf	Connection	Weight
very far	very low	25	And	1
very far	low	24	And	1
very far	medium	23	And	1
very far	high	22	And	1
very far	very high	21	And	1
far	very low	20	And	1
far	low	19	And	1
far	medium	18	And	1
far	high	17	And	1
far	very high	16	And	1
medium	very low	15	And	1
medium	low	14	And	1
medium	medium	13	And	1
medium	high	12	And	1
medium	very high	11	And	1
close	very low	10	And	1
close	low	9	And	1
close	medium	8	And	1
close	high	7	And	1
close	very high	6	And	1
very close	very low	5	And	1
very close	low	4	And	1
very close	medium	3	And	1
very close	high	2	And	1
very close	very high	1	And	1

Table 2 Fuzzy Inference functions methods

Method	Function
And	min
Implication	min
Aggregation	max
Defuzzification	centroid