

ARTICLE

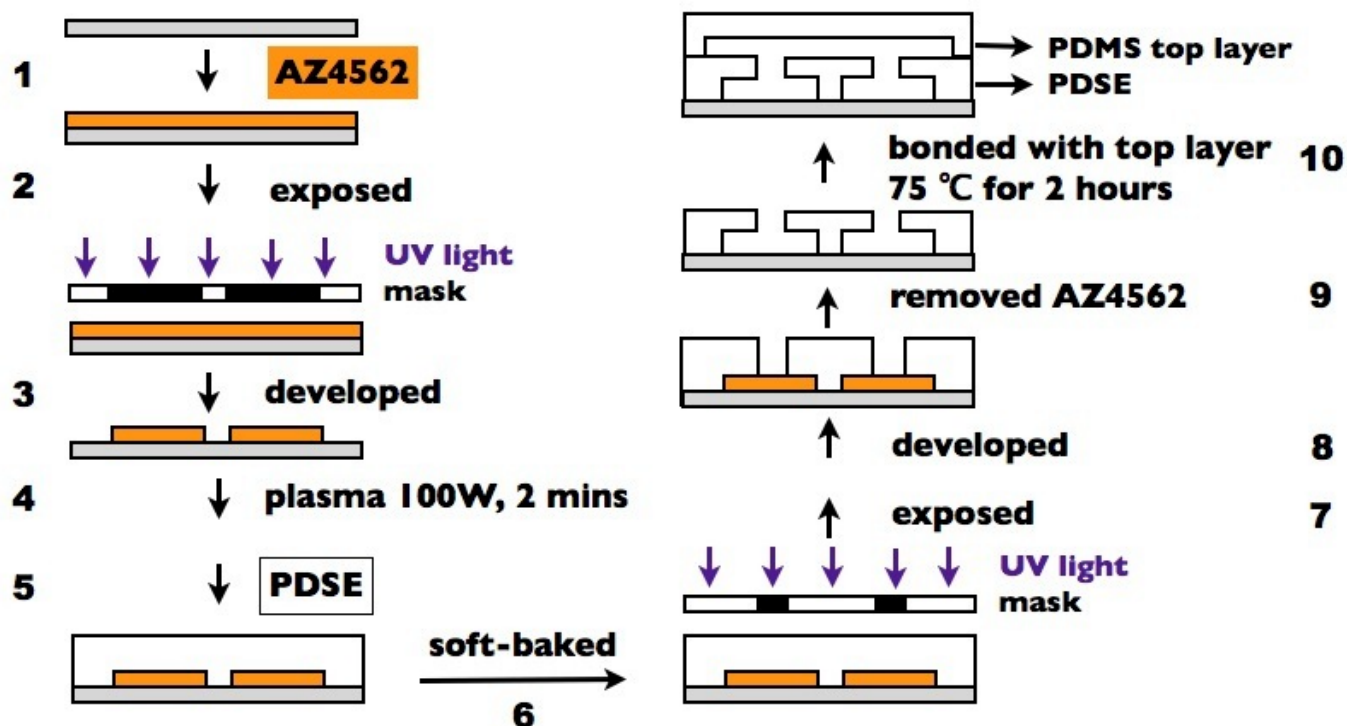
ESI (S1)

Detail of Fabrication

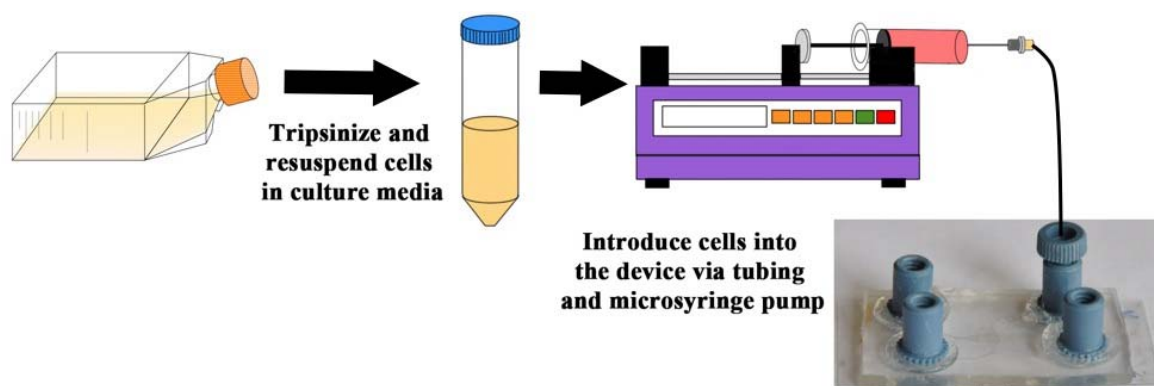
The circular cavities in the bottom of the devices were fabricated using standard soft lithographic techniques. In detail, a glass coverslip substrate was coated with AZ4562 positive photoresist by spinning at 4000 rpm for 30 sec to achieve a thickness about 6  $\mu\text{m}$ , soft-baked at 65°C for 5 min (hotplate) then 100 °C for 10 min (hotplate), exposed to UV light for 20 sec (144 mJ cm<sup>-2</sup>), and developed in AZ400K developer. Before fabricating the middle layer, the substrate was baked on a 127±3 °C hotplate for 2 min and was treated with oxygen-plasma for 2 min at a power of 100 W (Plasma Fab 5 from Gala Instrument) to facilitate the attachment of PDSE to the substrate.

The array of 40  $\mu\text{m}$  holes in the middle layer were fabricated by spreading PDSE (product number WL-5150 from Dow Corning) over the plasma treated substrate having the AZ4562 pattern. The PDSE layer was spun at 500 rpm for 55 sec with a ramp rate of 100 rpm s<sup>-1</sup> to give a thickness of about 29-32  $\mu\text{m}$  (measured using Dektak Profilometer). This was followed with a final spin at 750 rpm for 65 sec to reduce edge effects. Subsequently, the substrate was soft-baked at 65 °C for 90 sec, exposed for 90 sec (30 sec for 3 cycles with 5 sec waiting time) using soft contact and post-exposure baked at 127±3 °C for 90 sec (hotplate). The substrates were next developed in hexamethylsiloxane (Dow Corning) for 4 min and rinsed in isopropyl alcohol (IPA) and RO water, respectively. Prior to bonding the separately made top layer, the cavities and submerged channels on the bottom layer were developed by dissolving away the AZ4562 pattern using acetone in an ultrasonication bath for 1 min, and rinsing with RO water.

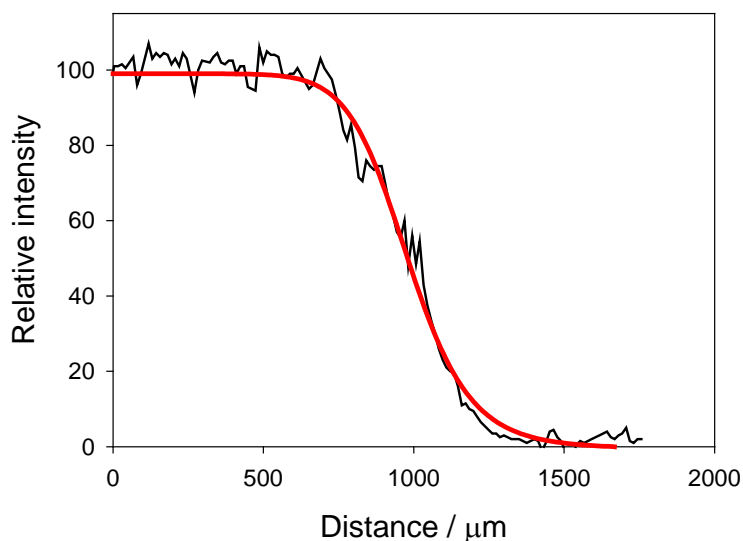
The upper layer part of the devices were made from partially cured PDMS (Dow Corning, Sylgard®184) using an elastomer to curing agent ratio of 20:1 w/w (cured at 75°C for 15 min). The texture of partially cured PDMS at this degree of curing is relatively plastic. The PDMS was peeled off from the moulds and the holes to form the inlet and outlet connections were punched with a flat ended needle (22G) prior to bonding to the middle and bottom layer by baking in a 75°C oven for a further 2 hours.



**ESI Figure 1** The VIA device fabrication process. Step 1-3 involved making the circular cavity and the submerged channel structure at the bottom with AZ4562 resist. Step 4-8 involved making an array of VIA using PDSE. Step 9 involved dissolving the bottom layer structures away with acetone. Step 10 involved assembly of the PDMS top layer with the PDSE device containing the array of microholes and submerged cavities.



**ESI Figure 2:** Schematic of the process for cell loading and studying cell response in the device.



**ESI Figure 3:** Estimation of .SDF-1 $\alpha$  gradient within the device of Figure 7 through use of fluorescein labeled dextran as a proxy for SDF-1 $\alpha$ . The inlet flow rates were  $0.05 \mu\text{l min}^{-1}$  with the dextran solution flowing into the uppermost port of the top layer, and PBS being flowed into the lowermost port of the top layer (see main Figure 1D). Both ports of the bottom layer served as the outlets. The profile above corresponds to a midline drawn top to bottom through the image of Figure 7E; the 'noise' in the measured fluorescence trace is due to undulations in the fluorescence signal caused by the presence of holes and other features in the device. The red line is a fit to the data using a sigmoidal curve. In regions of the device where the relative fluorescence intensity was 90-110, the concentration of SDF-1 $\alpha$  was assumed to be that of the bulk ( $100 \text{ ng ml}^{-1}$ ), and the SDF-1 $\alpha$  concentration was assumed to scale with the fluorescence intensity.