Electronic Supplementary Material (ESI) for Lab on a Chip.

Electrokinetic Study on Tunable 3D Nanochannel Networks Constructed by Spatially Controlled Nanoparticle Assembly

Eunpyo Choi, [1] Kilsung Kwon, [1] Daejoong Kim, [1,*] and Jungyul Park[1,*]

[1] Department of Mechanical Engineering, Sogang University, 35 Baekbeom-ro, Mapo-gu, Seoul, 121-742, Korea

S.I Fabrication process for PDMS microfluidic channels with multilayered design

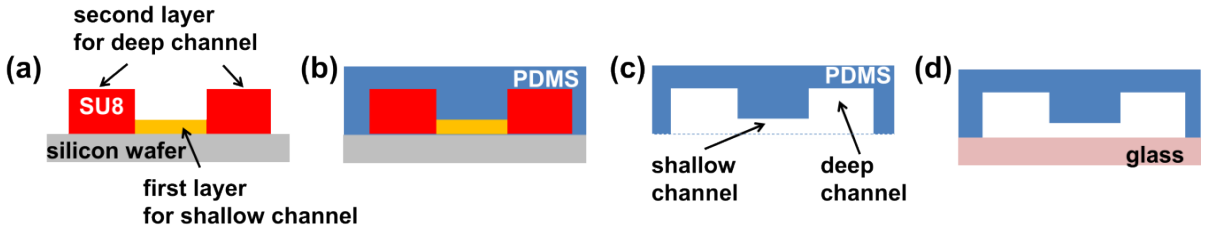

Fig. S1 Scheme of the fabrication process for PDMS microfluidic channels with multilayered design.

Fig. S1(a) - (d) shows schematic diagrams that describe the procedures for fabricating microfluidic devices with multilayered design. We fabricated microfluidic chips using the standard soft lithography:[1] (a) A 4-inch silicon wafer was spin-coated with negative photoresist (SU-8 2005, MicroChem Inc., target: 5 μm to 100 μm), and then the coated silicon wafer was soft-baked for several minutes. The wafer was exposed under a mask using an aligner and placed on a hot-plate for several minutes of post-exposure baking, followed by a short relaxation time. Post-exposure baking was followed by development at room temperature, after which the whole wafer was rinsed with isopropyl alcohol (IPA) to clean the residues from the wafer. Subsequently, SU-8 2050 was patterned on the first SU-8 layer (target: 100 μm, this layer is for the deep channel) with same process as above. (b) A Polydimethylsiloxane (PDMS) precursor (Sylgard 184 Silicone Elastomer, Dow Corning) and a curing agent were mixed at a ratio of 10 to 1, based on weight. Before the PDMS mixture was poured onto the fabricated master, the master was silanized with (tridecafluoro-1,1,2,2,-tetrahydrooctyl)-1-trichlorosilane (Sigma Chemical Co., St. Louis, MO, USA) to allow easier removal of the PDMS after curing. The PDMS mixture was poured onto the master and cured at 95 °C for 1 h. (c) Then, the cured PDMS channel was

peeled off from the master, cut and punched to connect microtubes. (d) The PDMS devices were directly bonded to a glass substrate without any surface treatment and then they were treated with oxygen plasma under 50 sccm of O_2 and 70 W for 40 s (Cute-MP, Femto Science, Korea).

S.II Reproducibility

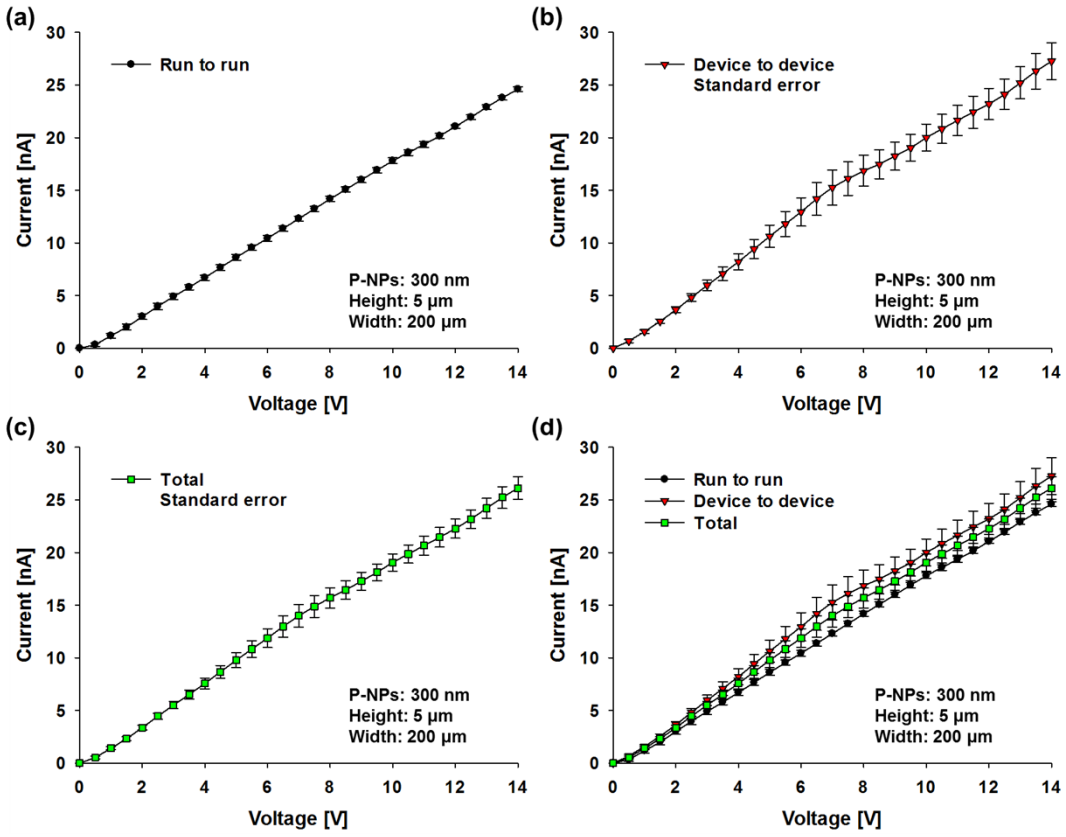

Fig. S2 *I-V* plots for describing (a) the run to run, (b) device to device, (c) total, and (d) overall immerged data with standard error bar.

Fig S2 (a), (b), (c), and (d) show the *I-V* plots for describing the run to run, the device to device, the total and the overall immerged data with standard error bar, respectively. The fixed condition is as follows; P-NPs: 300 nm, height of shallow channel: 5 μm, width of shallow channel: 200 μm. Each experiment was conducted 5 times and shown with standard error. The maximum standard error is ± 0.2870 nA for the run to run experiment and its value is much lower than the device to device case (±1.8809 nA). Based on these run to run and device to device reproducibility experiments, we re-plotted the total standard error bar as shown in Fig. S2(c). In this paper, all the *I-V* curves are plotted by using this total standard error.

S.III Evolution of the patterns of the ion depletion layer

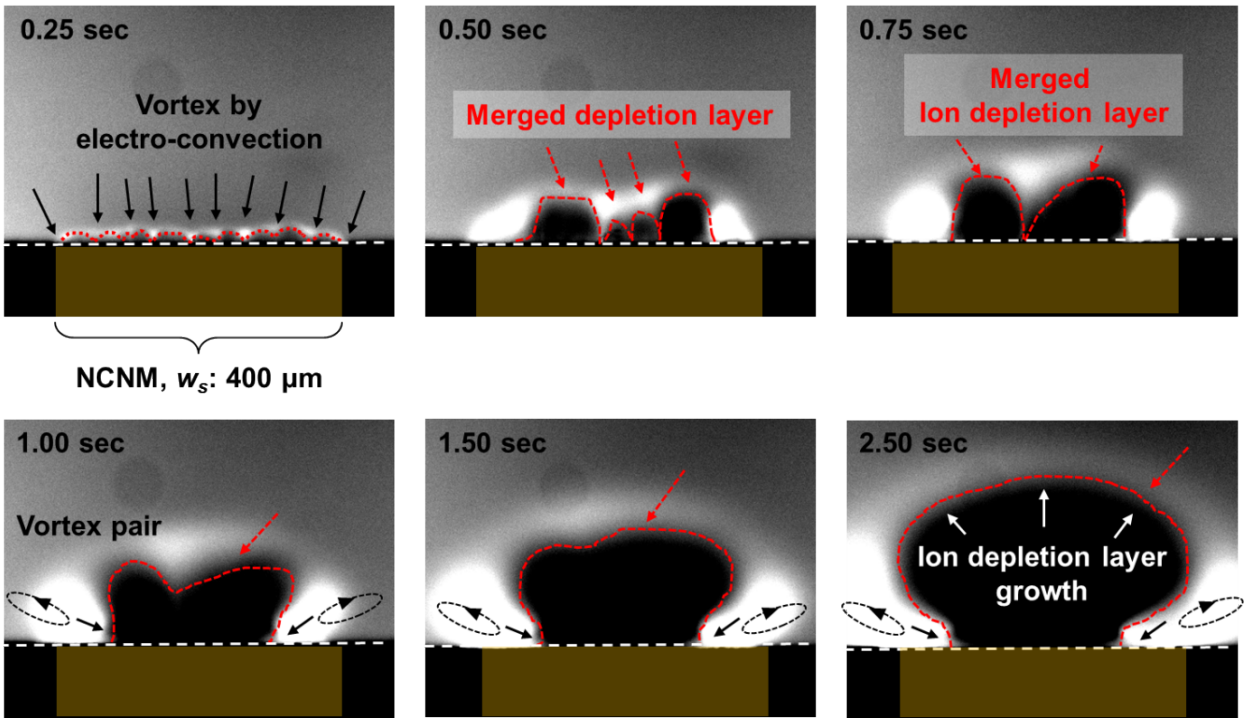

Fig. S3 Time sequence images of the depletion layer pattern evolution.

Fig. S3 shows the time sequence images of the depletion layer pattern evolution. In this case, we used the h_s with 5 um, w_s with 400 um, 300 nm of diameter of silica nanoparticles, 0.1 mM of KCl solution at value of pH 5.6 with FITC fluorescent dye, and +30 V of applied voltage. When the ICP were generated, small size of periodic undulation pattern of depletion layers were formed. Subsequently, these small layers became merged into one larger depletion layer and extended over time but there still existed ejecting vortices which disturb the stability of depletion layer at each side wall by the corner effects.[4]

S.IV Effective cross sectional area of ideally close-packed homogeneous nanoparticles into the FCC structure

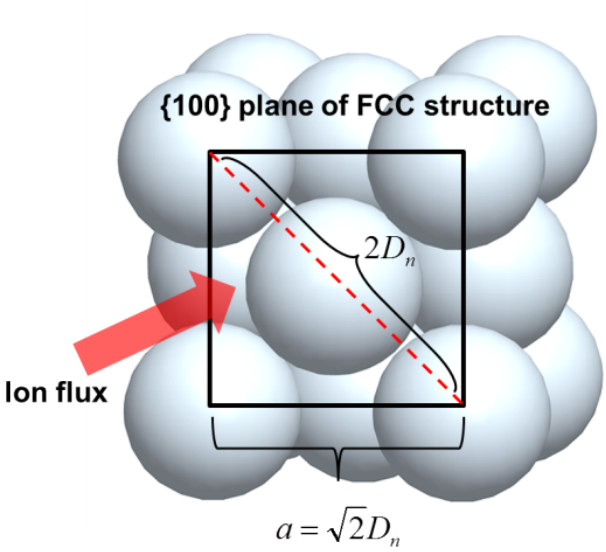

Fig. S4 Effective cross sectional area of ideally close-packed homogeneous nanoparticles into the FCC structure

Fig. S4 shows a unit of the effective cross section area (A_u^*) of the ideally close-packed homogeneous nanoparticles on the {100} plane of the FCC structure. A_u^* can be described as follows:

$$A_u^* = a^2 - 2\pi(\frac{D_n}{2})^2 \qquad \text{(S1)}$$

here, the former term, a^2, is the unit of the cross sectional area of the {100} plane and the latter term is the unit of the cross sectional area of the closed packed particles within the {100} plane. As substituting the $a = \sqrt{2}D_n$ for Eq. (S1), the A_u^* becomes following expressions:

$$A_u^* = (\sqrt{2}D_n)^2 - 2\pi(\frac{D_n}{2})^2 \approx 0.43{D_n}^2 \approx 0.215a^2 \qquad \text{(S2)}$$

Since the close-packed nanoparticle with FCC structure has the same packing efficiency, the ratio is insensitive to the width (w_s) and the height (h_s) of the shallow channel. In this reason, the effective cross sectional area of the shallow channel, A_s^*, can be estimated as $A_s^* = 0.215 w_s h_s$, i.e. 21.50 % of the A_s.

REFERENCES

1. E. Choi, H. K. Chang, C. Y. Lim, T. Kim and J. Park, *Lab chip*, 2012, 12, 3968-3975.