Supplementary Information

Morphological impact of zinc oxide layers on the device performance in thin-film transistors

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Transistor setup C

Besides the bottom-gate setups **A** and **B**, another setup **C** was employed to fabricate thin-film transistors based on spin coated ZnO nanoparticles. It consists of aluminium source and drain electrodes, a zinc oxide particle layer, 190 nm PVP dielectric and a gold top-gate electrode. As substrate materials a thermally oxidized silicon wafer was used as well as polyethylene naphtalane (PEN).

Transfer characteristics for devices on both subtrates are presented in Fig. S1, the extracted characteristic values are listed in table S1. Due to the top-gate architecture the devices exhibit an increased hysteresis as described recently.[31]

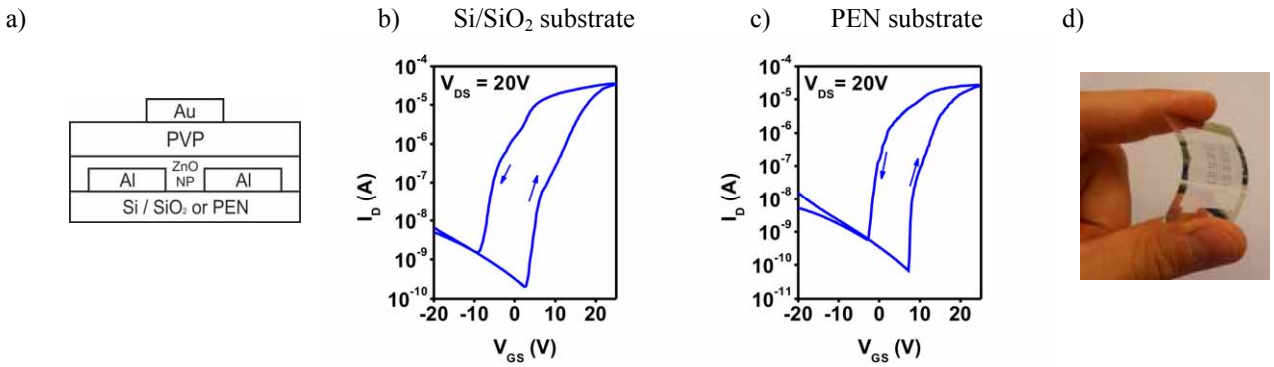

Figure S1: (a) Schematics of setup **C**. Transfer characteristics of TFT devices on (b) Si/SiO_2 and (c) PEN substrate. (d) Photograph of TFT array on flexible PEN substrate.

Table S1: Extracted TFT characteristics for ZnO particle based TFTs in device setup C on Si/SiO_2 and PEN substrates.

Substrate	**μ** $cm^2V^{-1}s^{-1}$	**V_{th}** V	**ON/OFF**	**I_D/I_G**
Si / SiO_2	**2**	**11.4**	**10^5**	**10^3**
PEN	**1.4**	**10.7**	**10^5**	**10^2**