Electronic Supplementary Material (ESI) for Nanoscale

Supporting Information

Fabrication and design equation of film-type large-scale interdigitated supercapcitor chips

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Experimental Details

A large-scale interdigitated supercapacitor chip based on a hierarchical MnO_2 structure was generated on a silicon wafer. The surface of the silicon wafer was wet oxidized to produce a silicon oxide layer (SHF-150, Seltron) and a positive photoresist layer was subsequently spin coated and developed on the oxidized layer using a photomask (MA-6, Karl-suss). A Cr layer and Pt layer were sequentially thermally evaporated onto the same layer as the adhesion layer and a supercapacitor current collector was applied (ALPS-C03, alpha plus). The hierarchical MnO_2 structure was electrodeposited on the surface of the Pt layer. For electrodeposition, the wafer was immersed in aqueous solutions of $Mn(NO_3)_2$ (0.02 M) and $NaNO_3$ (0.1 M) (WPG100, Wonatech).[15] The wafer was used as the working electrode, and a Pt electrode was used as the counter electrode, Ag/AgCl electrode used as the reference electrode, and a constant current of 100 $\mu A/cm^2$ was applied (15 – 120 min deposition time). After lifting off the photoresist with acetone followed by an overnight drying in a vacuum oven at 80 °C, a large-scale interdigitated patterned hierarchical MnO_2 structure was finally produced. For the full cell supercapacitor chip without an external electrolyte, a cover slip was attached to the fabricated supercapacitor chip and a 2 M Li_2SO_4 electrolyte solution was injected into the chip using microfluidics. Scanning electron microscopy images of the microelectrodes of the interdigitated supercapacitor chip were obtained using a field-emission scanning electron microscope (AURIGA, Carl Zeiss) and cyclic voltammograms of the interdigitated supercapacitor chips at various sweep-rates (10 mV – 5,000 mV) and a potential window of 0 V – 0.8V were analyzed (Iviumstat, Ivium).

Supplementary Figures

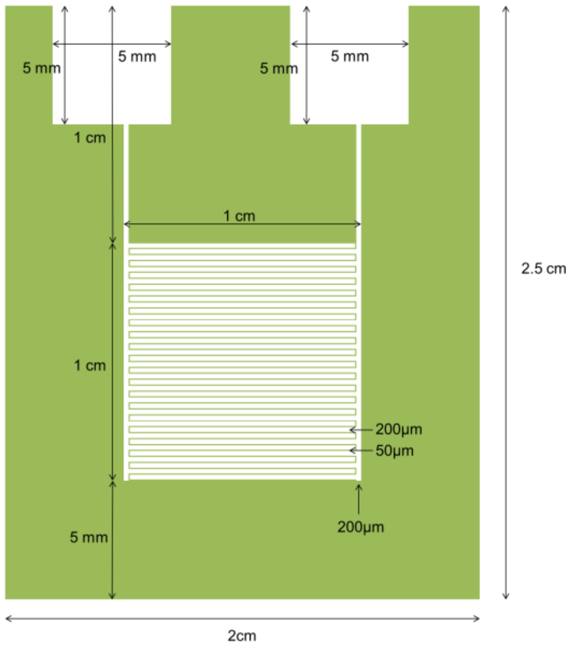

Fig. S1. Pattern design and linear dimensions of large-scale interdigitated supercapacitor chip with 40 interdigital electrodes. Each microelectrode was 200 μm in width and 1 cm in length. The electrodes were interspaced by 50 μm. Occupied area of the interdigital electrodes was 1 cm × 1 cm. This area can be increased up to the area limit of the electrochemical deposition method (size of counter electrode).

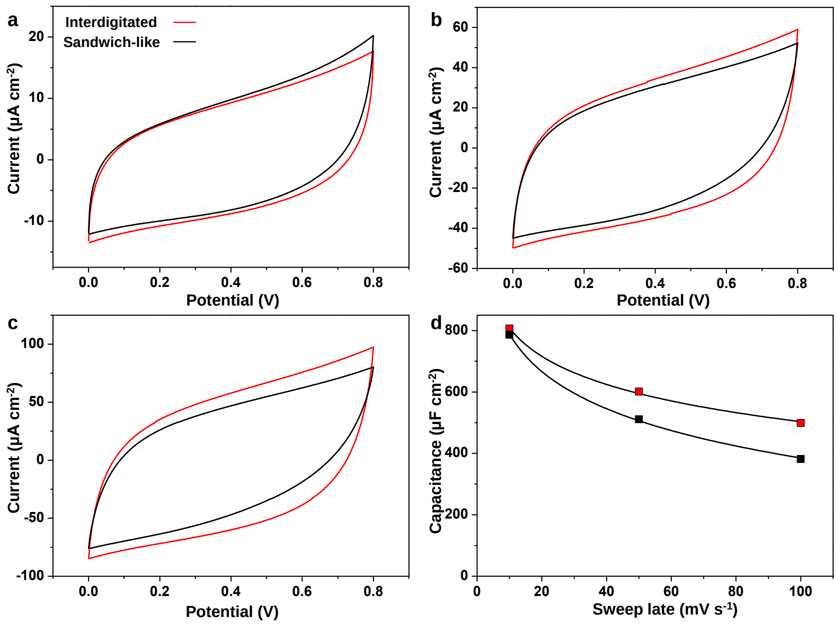

Fig. S2. (a), (b), (c), Cyclic voltammograms (CV) for large-scale interdigitated-supercapacitor chips and conventional sandwich type supercapacitors based on a hierarchical MnO_2 structure (60 min deposition time). Sweep rates were 10 mV s^{-1} (a), 50 mV s^{-1} (b), and 100 mV s^{-1} (c). (d) Capacitance versus sweep-rate for large-scale interdigitated supercapacitor chip and conventional sandwich-type supercapacitor based on a hierarchical MnO_2 structure. The electrolyte was a 2 M Li_2SO_4 solution at room temperature.

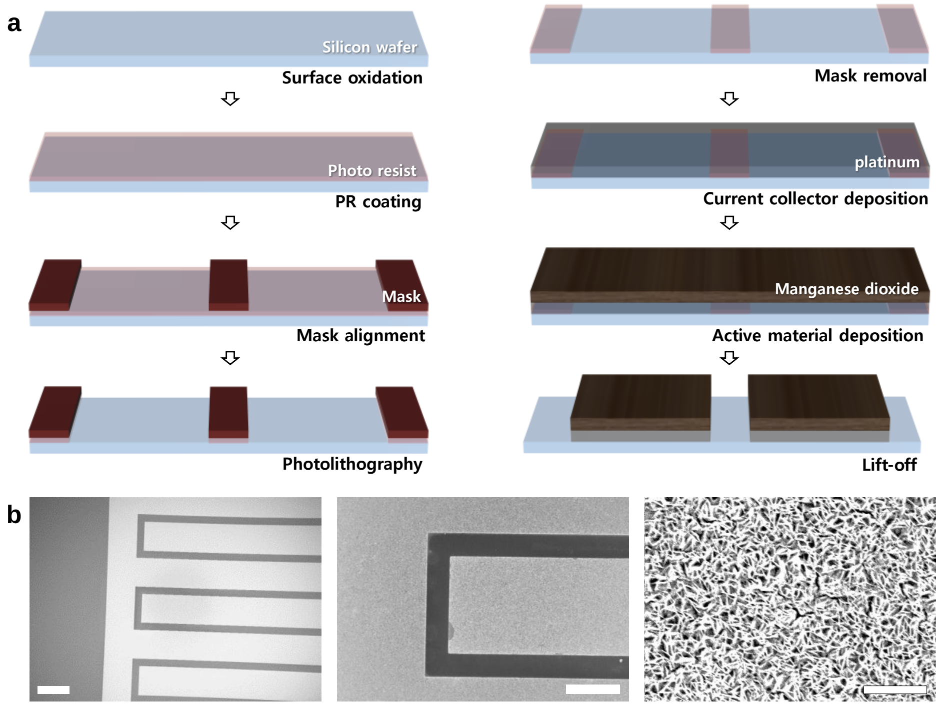

Fig. S3. (a) Details of the procedure used to fabricate a large-scale interdigitated supercapacitor chip based on a hierarchical MnO_2 structure microelectrode. (b) SEM images of the interdigitated patterned microelectrode based on a hierarchical MnO_2 structure (120 min deposition time) (scale bar : 200 μm, 100 μm and 5 μm).

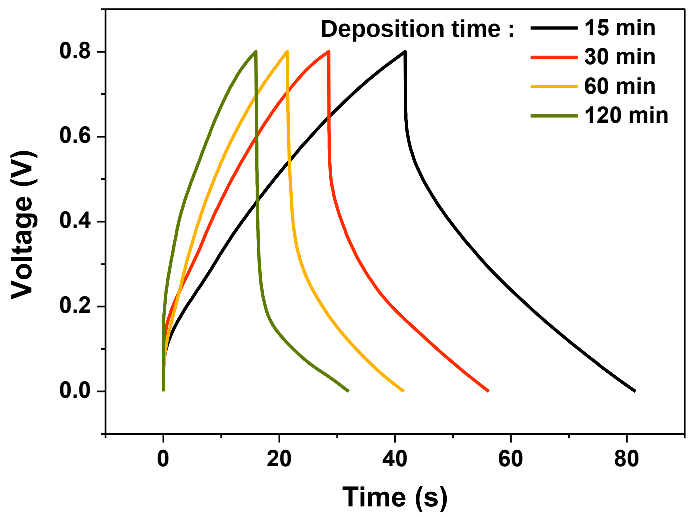

Fig. S4. Galvanostatic charge-discharge (voltage versus time) curves at four different deposition times. The deposition times for MnO_2 were 15 min, 30 min, 60 min, and 120 min, respectively. The current density was 40 μA per deposition time (h).

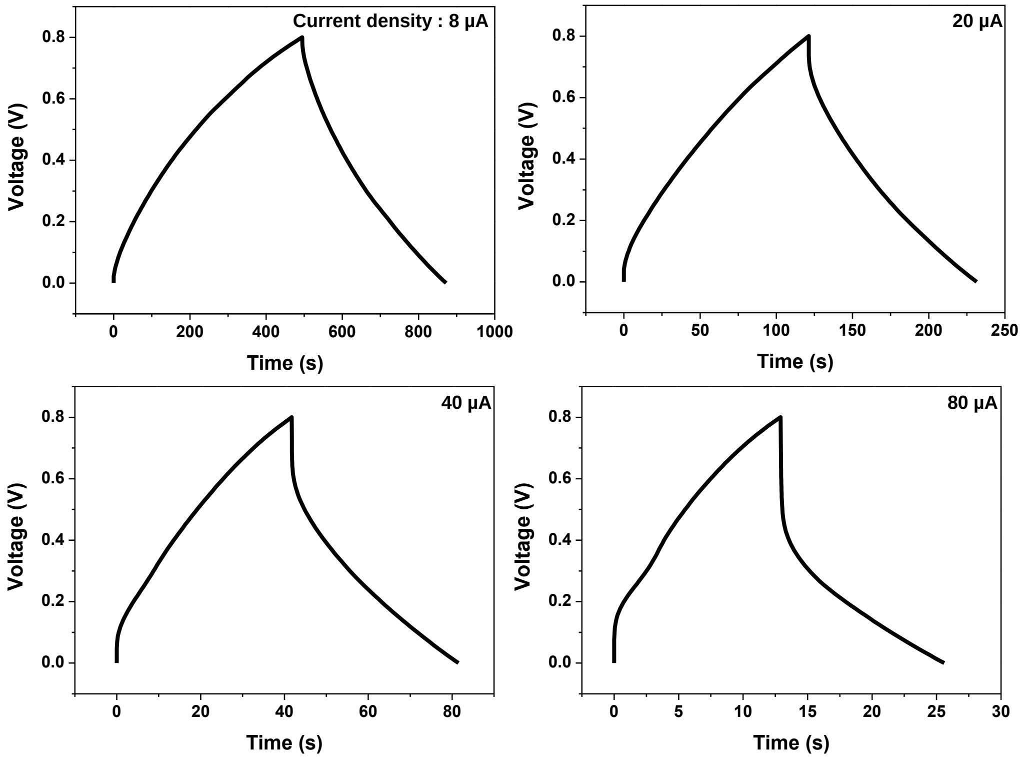

Fig. S5. Galvanostatic charge-discharge (voltage versus time) curves at four different current densities. The deposition time of MnO_2 was 15 min. The current densities were 8 μA, 20 μA, 40 μA, and 80 μA per deposition time (h), respectively.

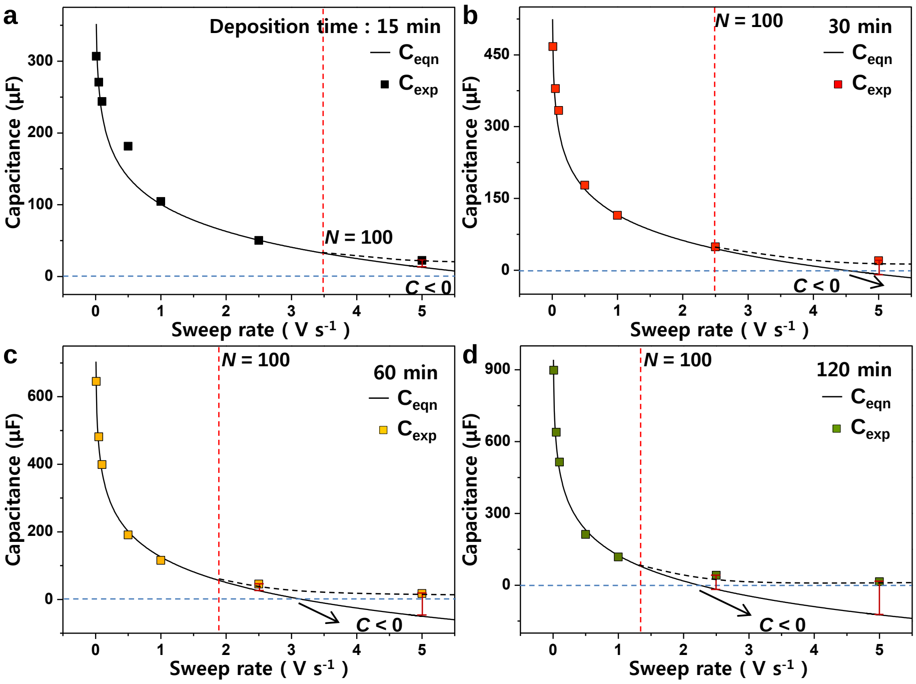

Fig. S6. Capacitance versus sweep-rate at the four different deposition times for correlation between calculated capacitance (C_{eqn}, line) and experimental capacitance (C_{exp}, point). C_{eqn} was estimated according to $C = -At^{1/2} ln(Bvt^{1/2})$, where A 1.82×10^{-6} F s^{-1} and B 5.26×10^{-3} V and C_{exp} at seven different sweep-rates between 10 and 5,000 mV s^{-1} and four different deposition times. The deposition times used were 15 min (a), 30 min (b), 60 min (c) and 120 min (d).

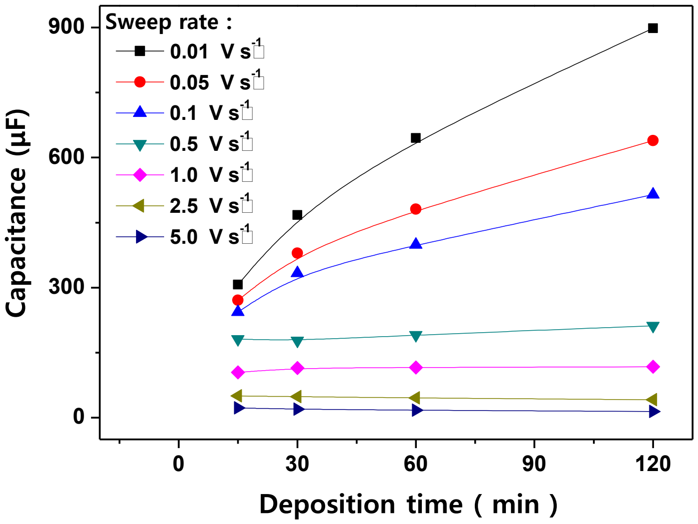

Fig. S7. Capacitance versus deposition time at seven different sweep rates. The sweep rates were 10 mV s^{-1}, 50 mV s^{-1}, 100 mV s^{-1}, 500 mV s^{-1}, 1,000 mV s^{-1}, 2,500 mV s^{-1}, and 5,000 mV s^{-1}.

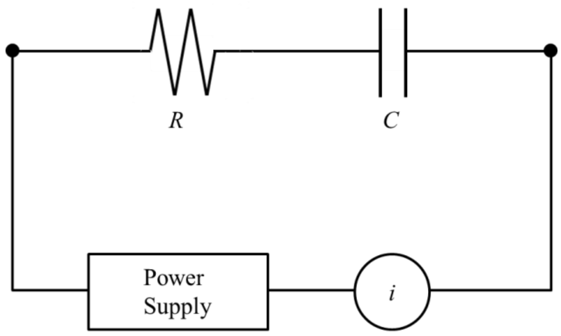

Fig. S8. Basic *RC* circuit for linear potential sweep method of supercapacitor system where *R* is resistance of equivalent circuit and *C* is capacitance. In this basic *RC* circuit, $\mathrm{E} = \mathrm{E}_R + \mathrm{E}_C = iR + q/C$ where E is potential, *q* is electrical charge. In linear potential sweep method, $\mathrm{E} = vt$ where *v* is sweep rate and *t* is discharge time, therefore these equations can be combined to $vt = R(dq/dt) + q/C$. In conclusion, if current attains a steady-state, $i = vC$ as is in equation (3) in the main text.[31]

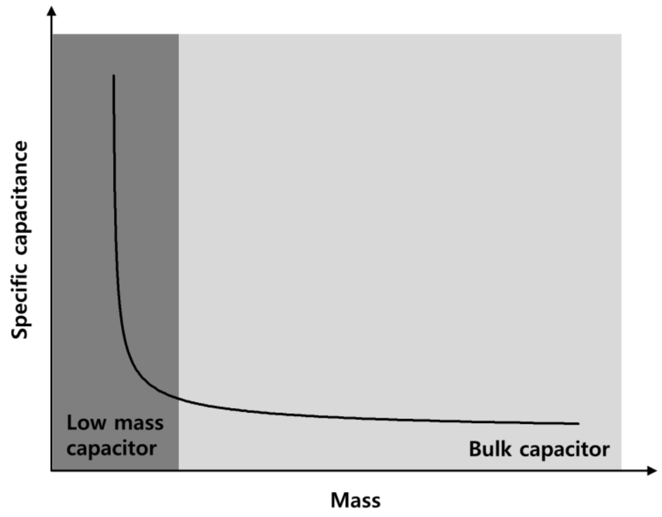

Fig. S9. Plot for specific capacitance versus mass calculated according to equation (10), $C_{sp} = -A'm^{-1/2}ln(B'vm^{1/2})$. The sweep rate was assumed to be constant.