SUPPLEMENTARY SECTION

Enhanced current-rectification in bilayer graphene with an electrically tuned sloped band gap

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1. *Device Fabrication:*

The bilayer graphene (BLG) flakes were obtained by micromechanical cleavage of Kish graphite, and deposited on a highly doped Si substrate with a 285 nm-thick SiO_2 layer. The flakes were identified by the contrast method of the optical reflection[1,2]. The patterning of the electrodes and of the graphene channel was performed by electron-beam (e-beam) lithography. For the e-beam lithography, we spin-coated two layers of resist, composed by MMA (8.5) copolymer and 950k-PMMA (both supplied by Nano™ MicroChem). The resists were developed with a 1:3 mixture of MiBK (Sigma-Aldrich) and isopropyl alcohol. After e-beam exposure and developing, it was formed an undercut space underneath the top layer resist. The deposition of the metals and patterning of the BLG channel were performed as follows:

1. The source-drain electrodes: Ti (5nm) and Au (50 nm) were deposited by thermal evaporation of the metal sources.
2. The patterning of BLG channel: an etching by oxygen plasma defined a channel with length about 28 μm and width about 4.7 μm.
3. The SiO_2 top-gate electrode: the undercut profile of the resist polymer was fundamental to make the sloped profile of the top-gate. The deposition of the SiO_2 by e-beam followed sequential angle evaporations, as it is showed in Fig. S1(a). The substrate was rotated around a fixed axis, from -20 to 20 degrees, with steps of 4 degrees. For each step, 1 nm of SiO_2 was deposited. Because of partial shading effect due to the undercut space underneath the top resist layer, the sloped SiO_2 top-gate is formed (Fig. S1(b)). The height of the SiO_2 top-

gate and the sloped-side region were determined by non-contact atomic force microscopy (Fig. S1(c)).

4. The AlO_x top-gate electrode on the BLG and on SiO_2 sloped top-gate: the 60 nm-thick Al layer was deposited by thermal evaporation. According to Miyazaki *et al*[3,4,5], even the surface of Al in contact with the BLG or SiO_2 was oxidized, and the AlO_x layer on the top of the BLG was used as top-gate contact.

After each deposition of metal, the lift-off process was performed using acetone and isopropyl alcohol.

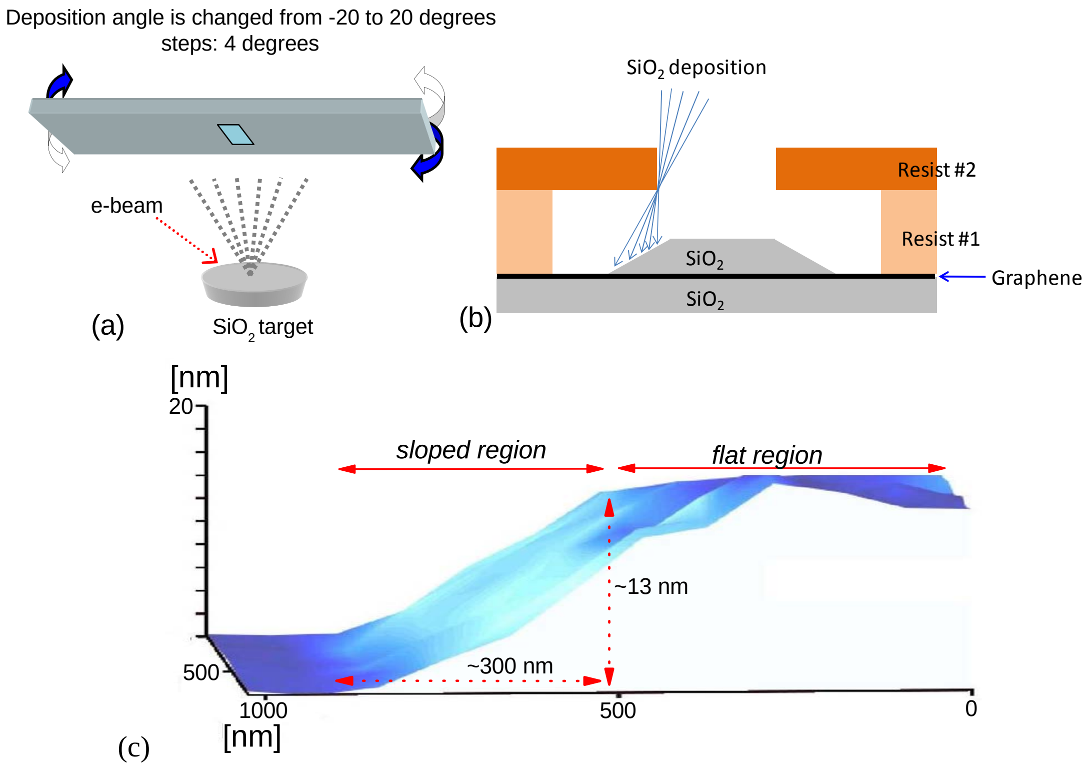

Fig. S1: (a) Deposition method of the SiO_2 top-gate. The deposition angle was changed from -20 to 20 degrees in steps of 4 degrees. (b) Schematic figure showing the undercut space underneath the top layer resist and the formation of the sloped SiO_2 top-gate (c) AFM image of the sloped SiO_2 top-gate electrode, showing the height and the sloped side region.

2. *The widening of the insulating region between p and n regions in sloped junctions:*

According to our previous report by Miyazaki *et al*[4], in the gate-controllable *pn* junctions, the depletion region is neutrally charged. This occurs due to a transient region around the *pn* interface where the top electrical field changes from an E_{tn} to E_{tp}

value. Usually, the transient region width determines the depletion region[4]. In case of an abrupt junction, the top-gate electrical fields changes abruptly in the interface, leading to a narrow transient region.

For sloped junctions, the top-electrical field changes smoother between *p* and *n* areas. The transient region is larger than in the abrupt junction, and the charge concentration is zero at a larger range around the *pn* interface, leading to a wider depletion region in sloped junctions.

References:

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