

## Supplementary Information

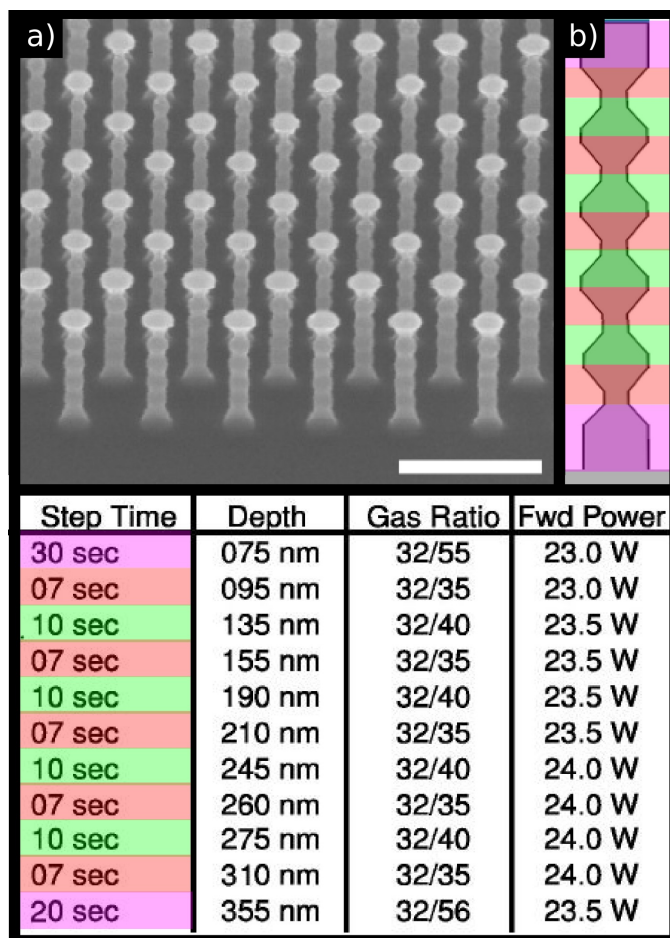
The fabrication in this paper was done on 2 in. prime, (100), 1-10 ohm-cm resistivity *n* or *p* type silicon wafers.

**Patterning:** The patterns were written with a Leica 5000+ electron beam pattern generator (EBPG) into MicroChem PMMA A3 950k electron beam resist. Following resist development aluminum oxide was deposited via reactive sputter deposition at 10 mTorr, 400 W DC forward power and a 5:1 Ar : O<sub>2</sub> gas ratio. The pattern was transferred via lift-off in dichloromethane with a 30 second soak and a 30 second sonication.

**Etching:** Individual samples were affixed to carrier wafers for insertion into the etchers with MicroChem PMMA A4 950k and baked for 30 seconds to drive out solvents. The etching was conducted in an Oxford Plasmalab 100 ICP-RIE 380. Gas pressure within the chamber during the etch was 10 mTorr. For the vertical etch, forward (RIE) power was 23 W and ICP power was 1200 W. The gas flow-rates for SF<sub>6</sub> and C<sub>4</sub>F<sub>8</sub> were 32 and 55 sccm, respectively. As mentioned in the text the forward power and gas flow-rates were modified to achieve side-wall sculpting.

**VNPFET:** The nanopillar was etched into *p*<sup>+</sup> silicon (.005 ohm-cm) using a 50 nm disk of aluminum oxide and undercut to have a diameter of about 30 nm. After oxidation the silicon channel was approximately 15 nm in diameter and was surrounded by 10 nm of thermal oxide. Tungsten was deposited via DC sputtering in an Ar atmosphere at 10 mTorr and 200 W. A gate was defined using optical lithography and the tungsten was etched using SF<sub>6</sub> in an RIE. The vertical extent of the gate was defined by spinning on PMMA to a certain height and then using an SF<sub>6</sub> plasma to remove the tungsten from the sidewalls. The insulating layer was silicon dioxide deposited using a plasma enhanced chemical vapor deposition (PECVD) system with SiH<sub>4</sub> and N<sub>2</sub>O as the gaseous precursors. The upper portion of the oxide cladding was removed with buffered hydrofluoric acid masked with a layer of PMMA that would determine the vertical extent of the oxide removal. The top and bottom contacts were Ti, also deposited with DC sputtering (10 mTorr and 200W) and patterned with optical lithography and an SF<sub>6</sub> RIE. Testing was carried out with a home-built, computer controlled electronic probe station. Voltages were applied with a National Instruments USB NI-DAQ and current was measured with a picoammeter (Keithley 6485).

**Etching Identical 'Beads':** This etch was carried out by decreasing the passivation gas flow and oscillating it between two under-passivated states to widen and narrow the pillar. Every two oscillations the forward power is increase 0.5 W to counter-balance the spread in IAD and maintain identically sized 'beads.'



**Fig. 6** Etch recipe for multiple identical beads carved on a silicon nanopillar. A) Array of silicon pillars with a 50 nm bead in a 100 nm diameter pillar. Scale bar is 500 nm. B) Schematic of pillar with the various etch steps highlighted and the conditions are described in the table. Note that the steps with less passivation are shorter since the lower the flow of passivation gas the faster the etch progresses into the silicon. Therefore the 7s low, 10s high passivation steps etch will fabricate symmetric beads.