Electronic Supplementary Information

Long Single ZnO Nanowire for Logic and Memory Circuits: NOT, NAND, NOR Gate, and SRAM

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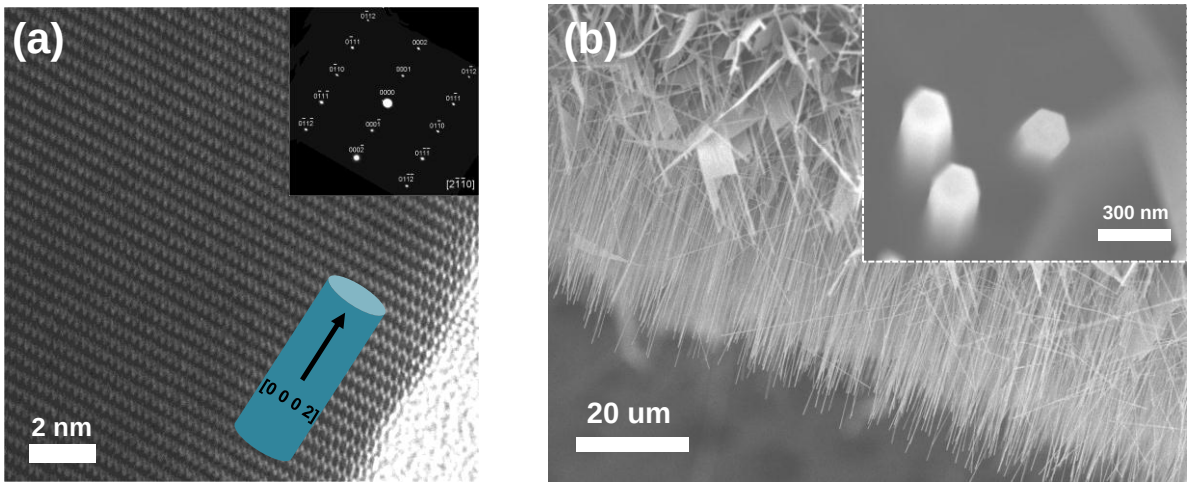

Fig. S1 (a) High resolution transmission microscopy (HRTEM) image for ZnO nanowires of ~100 nm in diameter. Selective area electron diffraction (SAED) pattern indicates that the growth direction of the single crystalline nanowire is [0002] (b) SEM images of as-grown ZnO nanowires on sapphire. From such nanowire forest we found 100 μm-long wires. Top view of the single crystalline nanowires is also shown in the inset (see the haxagons representing a single crystalline feature of NWs).

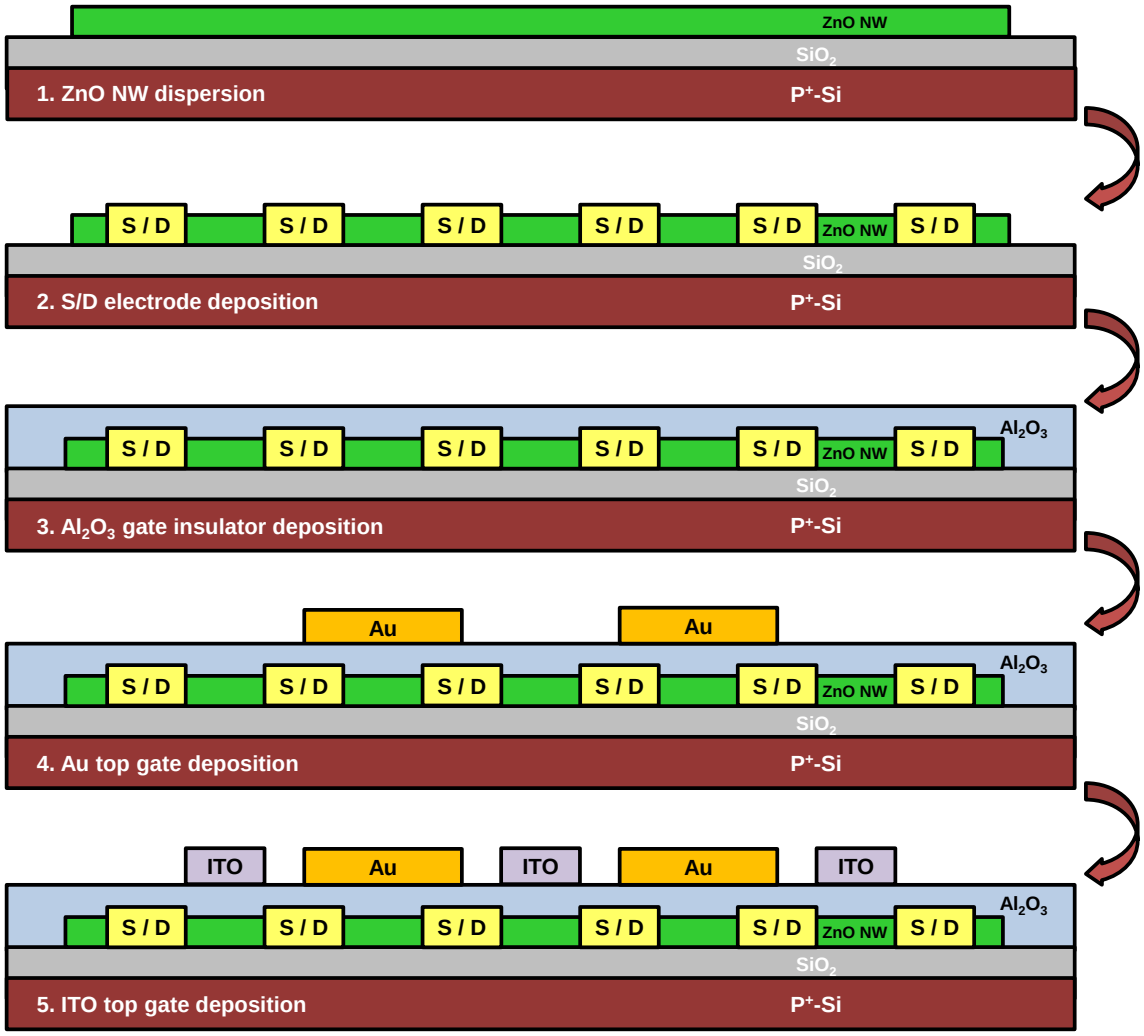

Fig. S2 Device fabrication steps illustrated in schematic cross-sectional view. 1. ZnO NW dispersion (drop and dry method). 2. S/D electrodes deposition (photolithography and lift-off process). 3. Al_2O_3 gate insulator deposition (ALD process). 4. Au top gate deposition (photolithography and lift-off process). 5. ITO top gate deposition (photolithography and lift-off process).

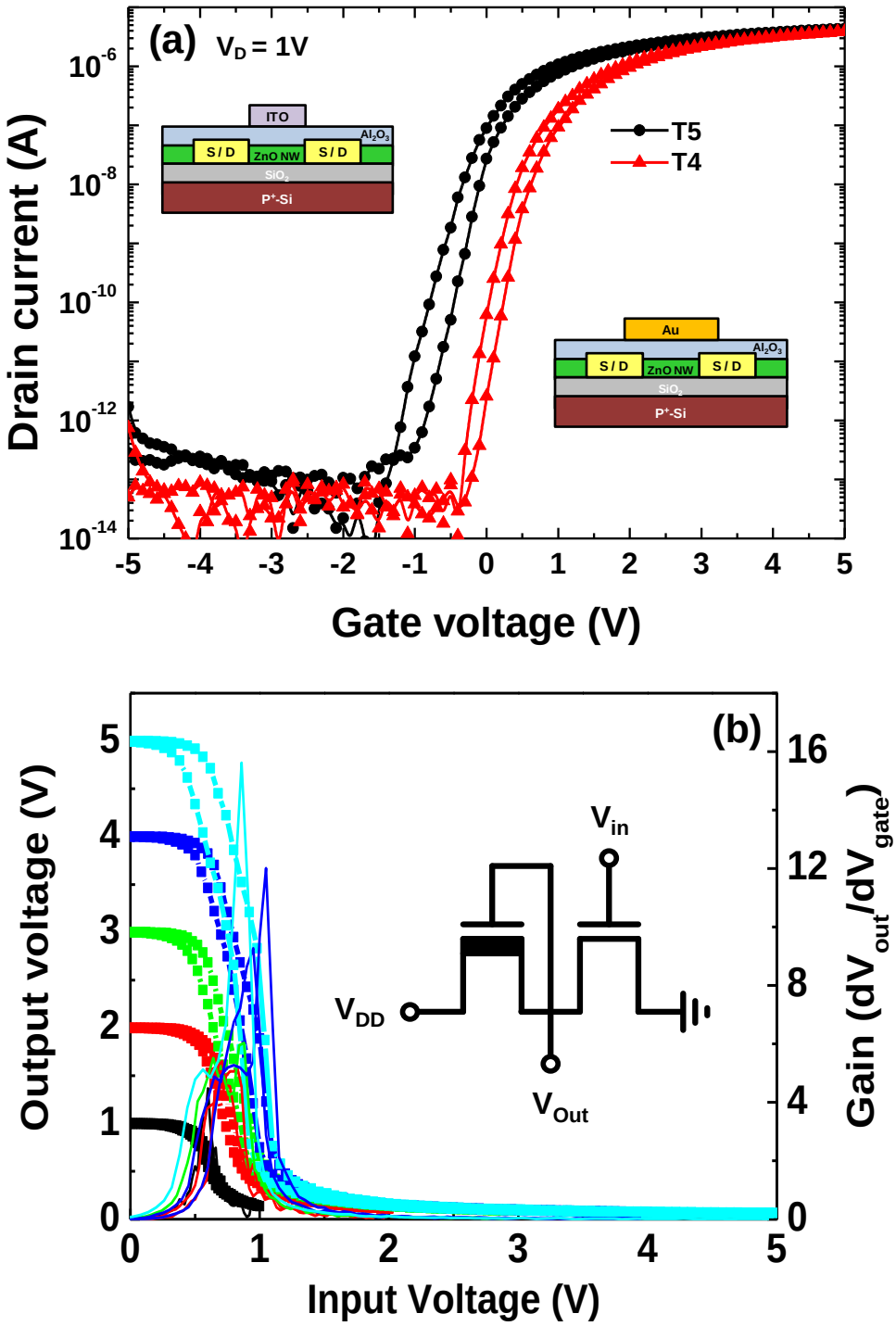

Fig. S3 (a) Transfer curves of two FETs formed on the different location of the same NW: T4 (Au gate) and T5 (ITO gate). Insets are the cross section schematics of T4 (right) and T5 (left). (b) VTC curves obtained from our inverter cell with T4 (driver) and T5 (load); the inset is the inverter circuit.

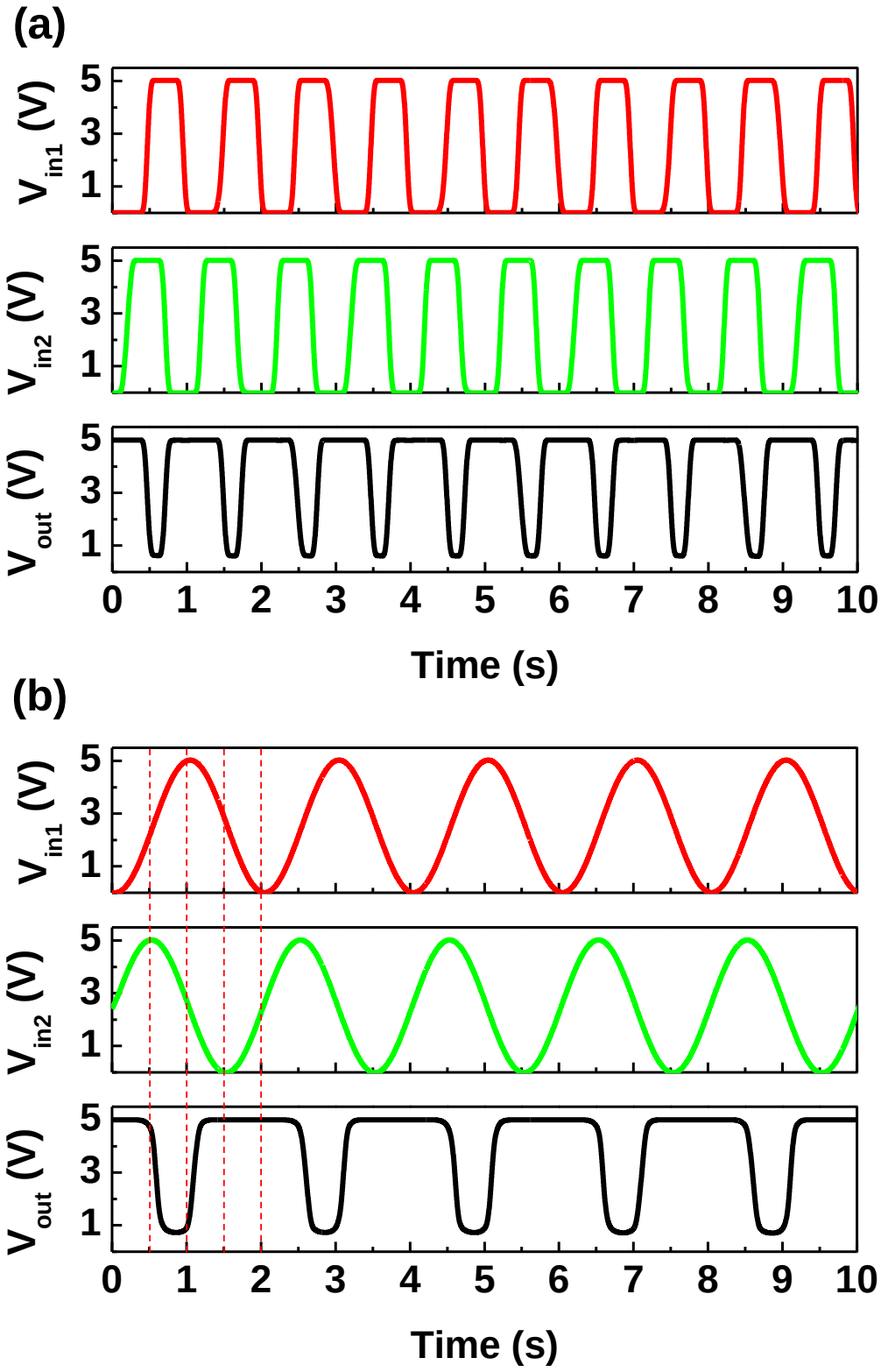

Fig. S4 Operation of ZnO NW-based NAND logic circuit. a) VTC output dynamics achieved from 1 s period square wave input pulses using V_{in1} and V_{in2}. b) VTC output dynamics achieved from two sine wave input voltages (2 s period).

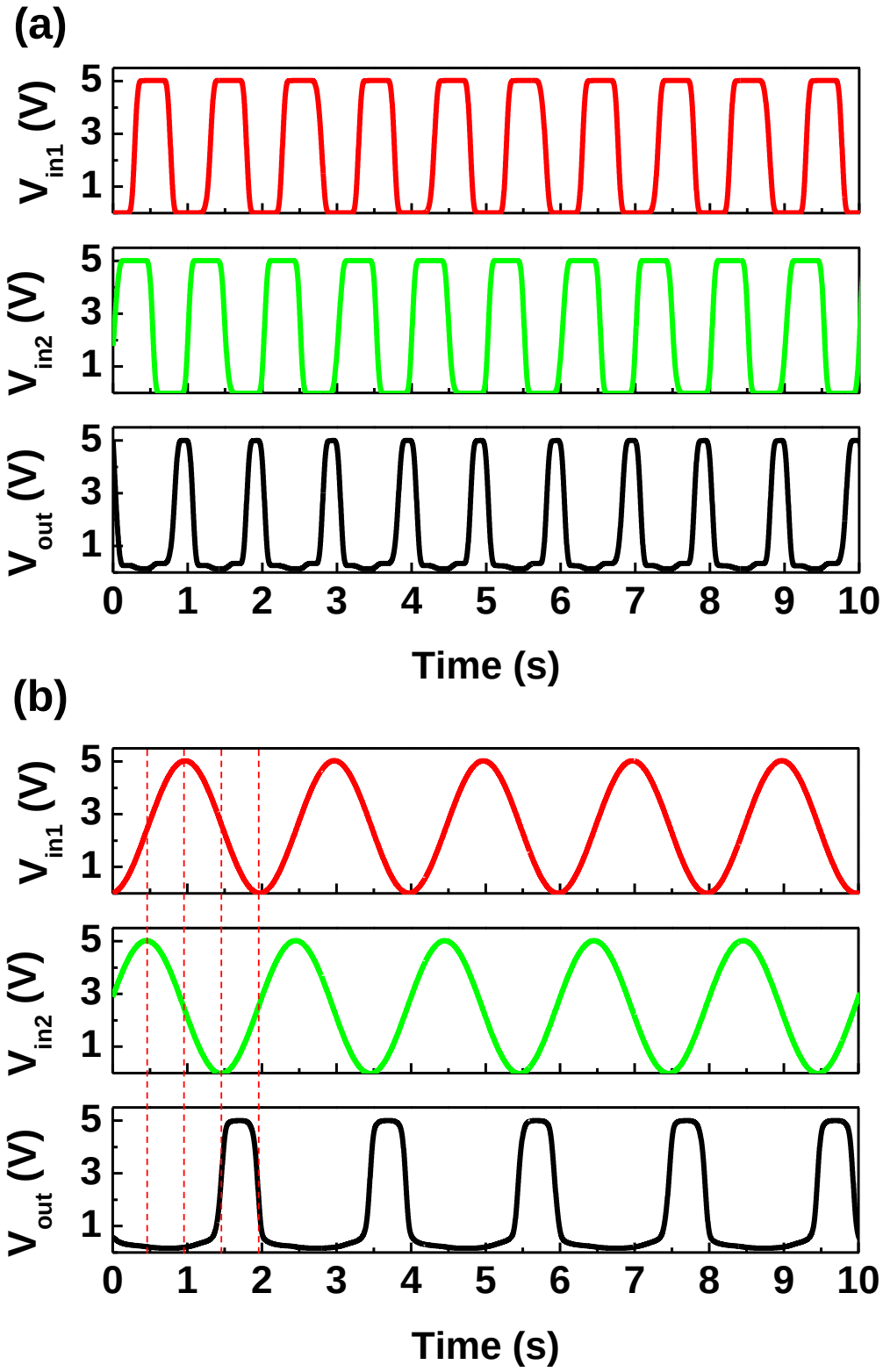

Fig. S5 Operation of ZnO NW-based NOR logic circuit. a) VTC output dynamics achieved from 1 s period square wave input pulses using V_{in1} and V_{in2}. b) VTC output dynamics achieved from two sine wave input voltages (2 s period).

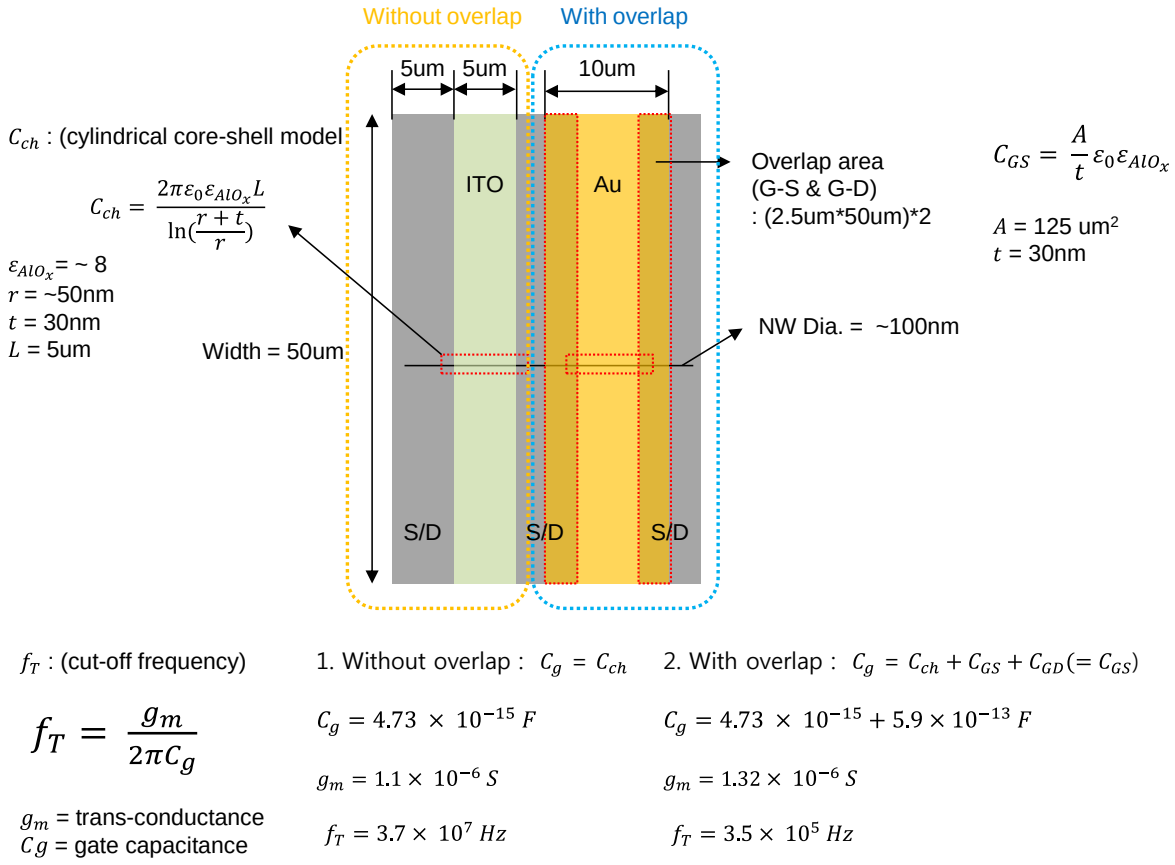

Fig. S6 Device schematic of cut-off frequency calculation model for ZnO NW FETs.

Above shows our inverter scheme including two ZnO NW FETs with ITO and Au gate, where Au gate makes some overlap capacitance unlike ITO gate. It is fact that the overlap reduces the cut-off frequency (f_T) of NW FET, so here we tried to calculate such f_T reduction effects by overlap. Now, the gate/source and gate/drain contact overlap is 2.5 μm each side and the overlap capacitance (C_{GS} = C_{GD}) of Al_2O_3 is calculated to be 2.95×10^{-13} F (so the total overlap cap. would be 5.9×10^{-13} F). The Al_2O_3 capacitance for gate/ZnO active channel (C_{ch}) is calculated to be 4.73×10^{-15} F, according to cylindrical core-shell model. This overlap capacitance is 125 times larger than without overlap area; thus the cut-off frequency of Au gate NW transistor is estimated to be 3.5×10^{5} Hz, which is 105 times smaller than ITO gate transistor. (Please consult with above drawing and numbers for more details).