Electronic Supplementary Material (ESI) for Nanoscale


Supporting Information to:

# High-performance Top-gated Monolayer $SnS_2$ Field-effect Transistors and Their Integrated Logic Circuits

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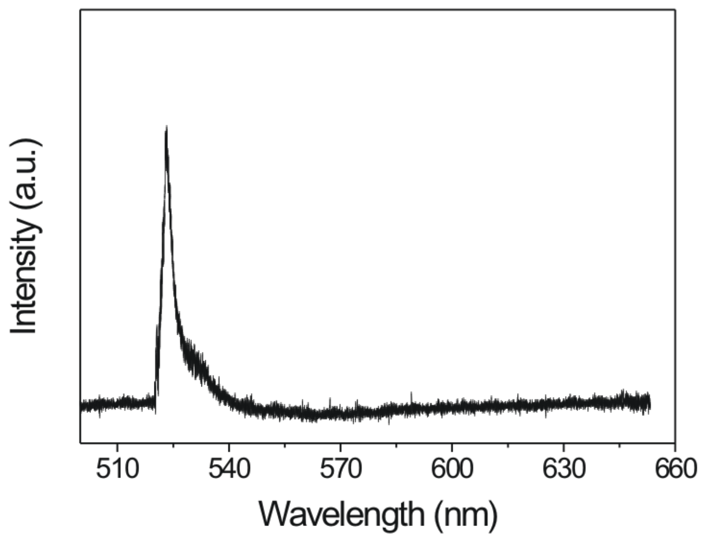


**Figure S1**. Micro-photoluminescence of single layer $SnS_2$ flake fabricated for TG-FET.

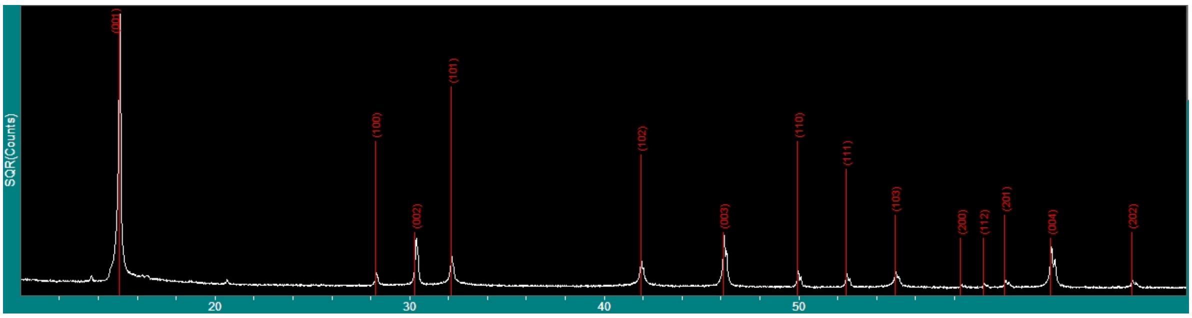


Figure S2. Powder XRD of $SnS_2$ bulks, red lines denote from the standard card and the white peaks correspond to XRD data. The exfoliated source demonstrates pure hexagonal $SnS_2$ with JCPDS NO.83-1706.

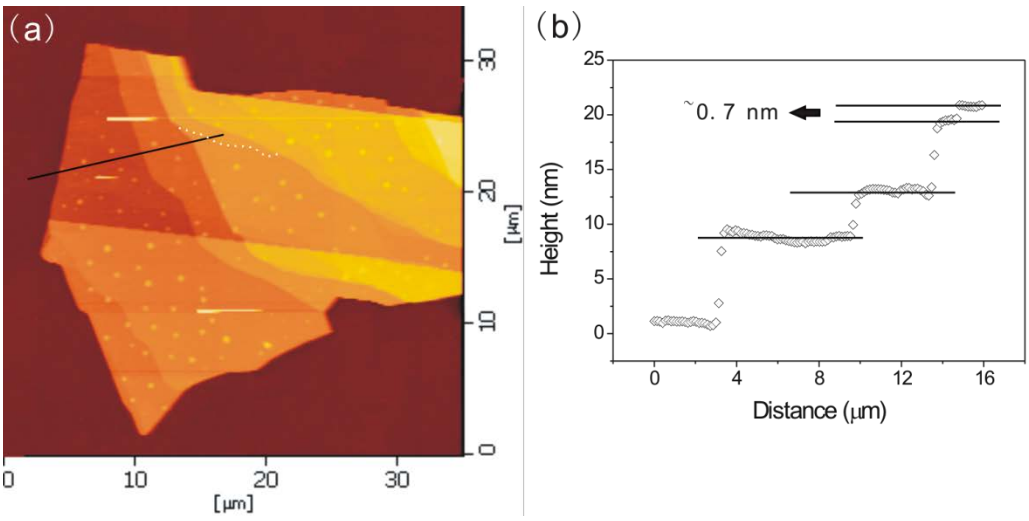


Fig.S3 (a,b) AFM image of multiple layer $SnS_2$ flake and its height profile along the black line. The white dotted line shows the boundary of two neighbor layers and the height difference is ~0.7 nm. The 0.7 nm scanning demonstrate that our AFM instruments can identify monolayer scanning.

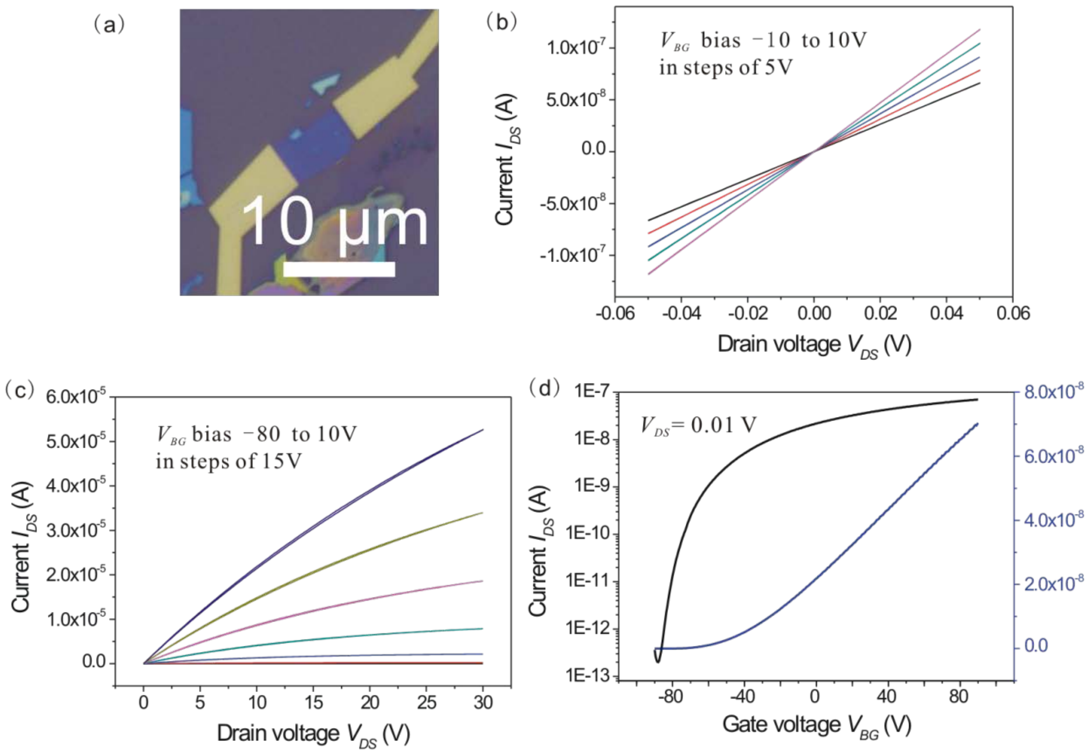


Figure S4. BG-FET performances with bare top surface, the carrier mobility is ~10 $cm^2$/Vs.

For the calculation to the BG-FET mobility: The BG-FET was measured in standard back-gated FET structure utilizing 285 nm $SiO_2$ covering layer with bare $SnS_2$ flake top surface as the channel. For the calculation of mobility, we utilize the linear working zone of FET as $\mu_{BG} = g_m \times \frac{L}{W} \times \frac{1}{C_i} \times \frac{1}{V_{DS}}$, while the transconductance $g_m = \frac{dI_{DS}}{dV_{BG}}$ was extracted from Fig. S2d, $g_m = 8\times10^{-10}$ A/V; the capacitance per unit area of $SiO_2$, $C_i = \varepsilon_0 \varepsilon_r / d = 8.85\times10^{-12}$ F/m×3.9 /(285×$10^{-9}$ m)=1.21×$10^{-8}$ F/$cm^2$; The ratio of channel length to width is ~5/3. Substituting all the above data, we can get $\mu_{BG} = g_m \times \frac{L}{W} \times \frac{1}{C_i} \times \frac{1}{V_{DS}} = 8\times10^{-10} \times \frac{5}{3} \times \frac{1}{1.21\times10^{-8}} \times 100$ $cm^2$/Vs ~10 $cm^2$/Vs.

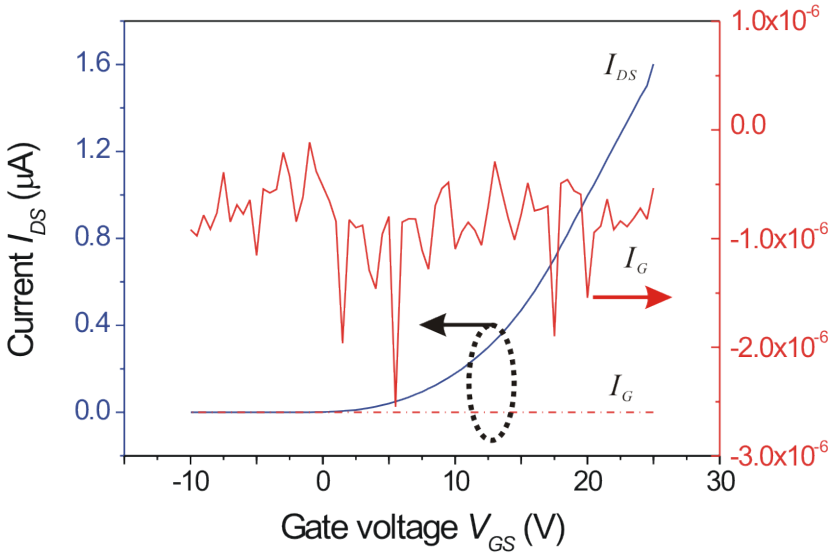


**Figure S5**. Leakage current ($I_G$) stands in the order of $10^{-14}$-$10^{-12}$ ampere during our measurement.