Electronic Supplementary Information for

A facile route for Si nanowire gate-all-around field effect transistor with steep subthreshold slope

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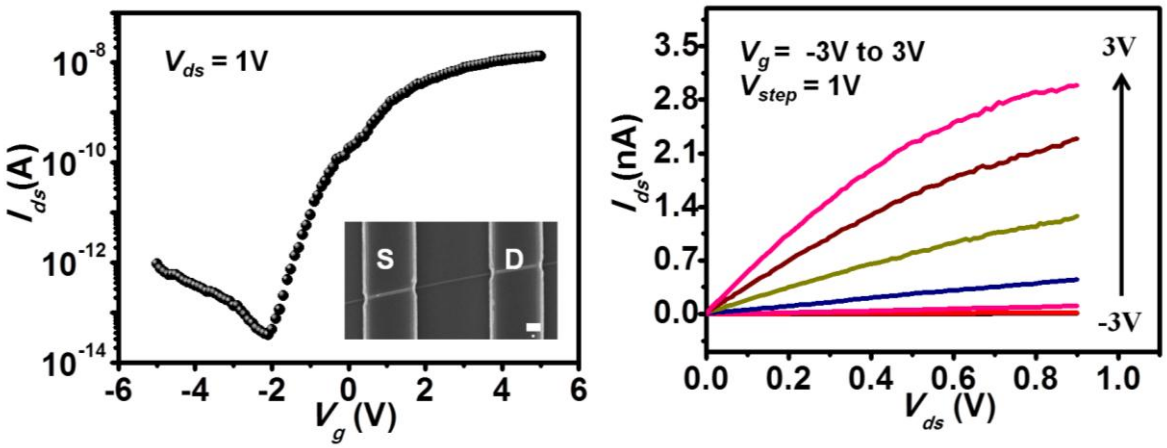

Fig. S1 (a) SEM image of SiNW planar FET; scale bar: 1 μm (b) Current-voltage (I_{ds}-V_{ds}) characteristics measured SiNW FET at various V_g.

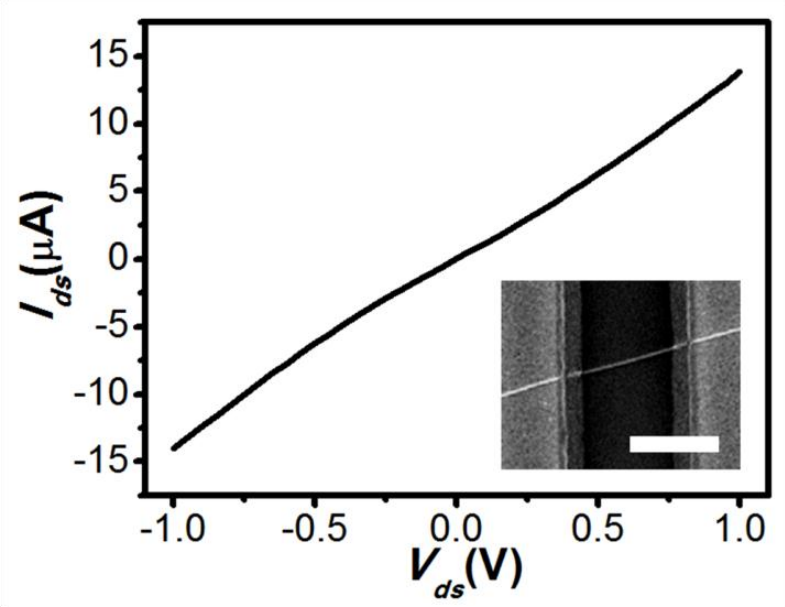

Fig. S2. Electrical conductivity of N^{++} Si shell. Inset shows SEM image of the $Si/SiO_2/N^{++}Si$ NWs device; scale bar = 5μm. For checking the electrical conductivity of $N^{++}Si$ shell, we fabricated $Si/SiO_2/N^{++}Si$ core shell NW device without additional etching of $N^{++}Si$ shell.

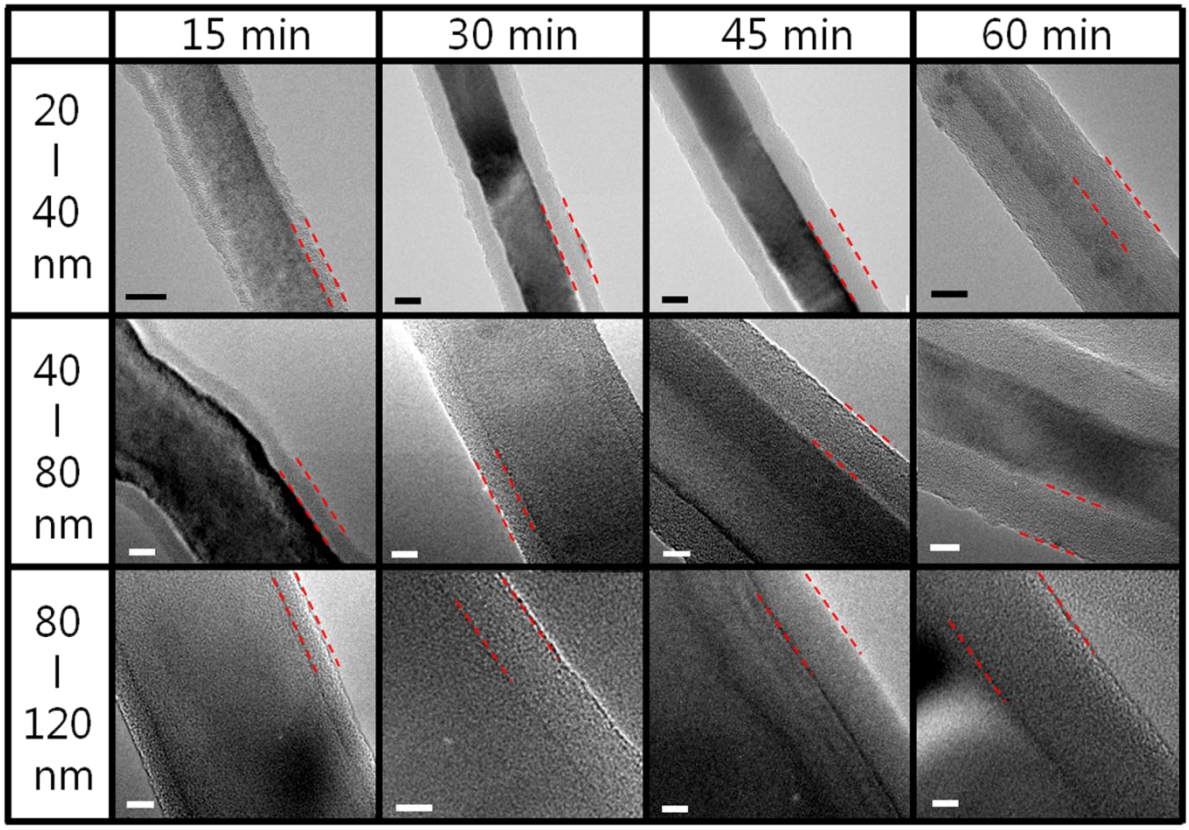

Fig. S3. Representative TEM images of Si/SiO_2 core/shell NWs with different diameter and oxidation time at 800 ^{o}C; scale bar = 10 nm

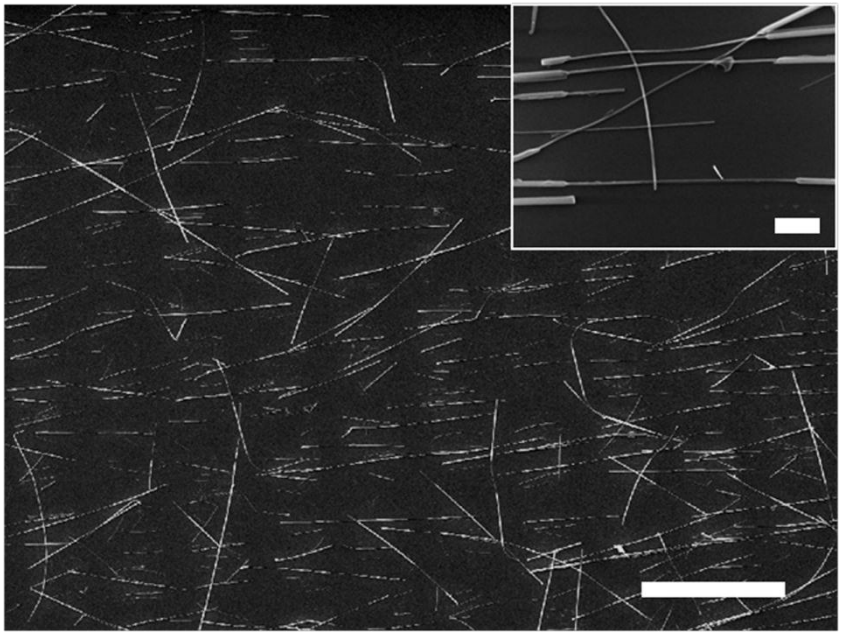

Fig. S4. (a) SEM image Si/SiO_2/N^+Si core/multi-shell NWs array after selective wet etching of N+ Si shell; scale bar = 10 μm, scale bar in the inset = 1 μm.

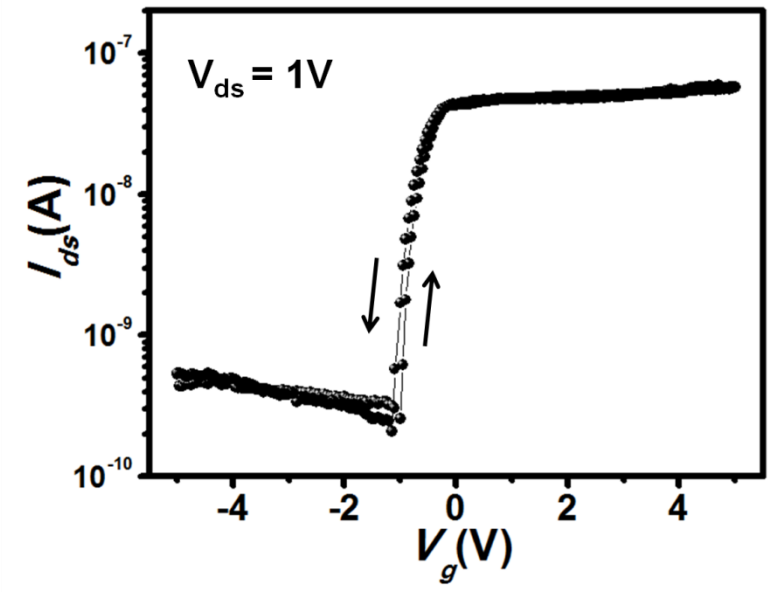

Fig. S5. Transfer characteristics (I_{ds}-V_g) of the SiNW GAA FET #2. Relatively small on/off current ratio is due to leakage current through gate oxide.

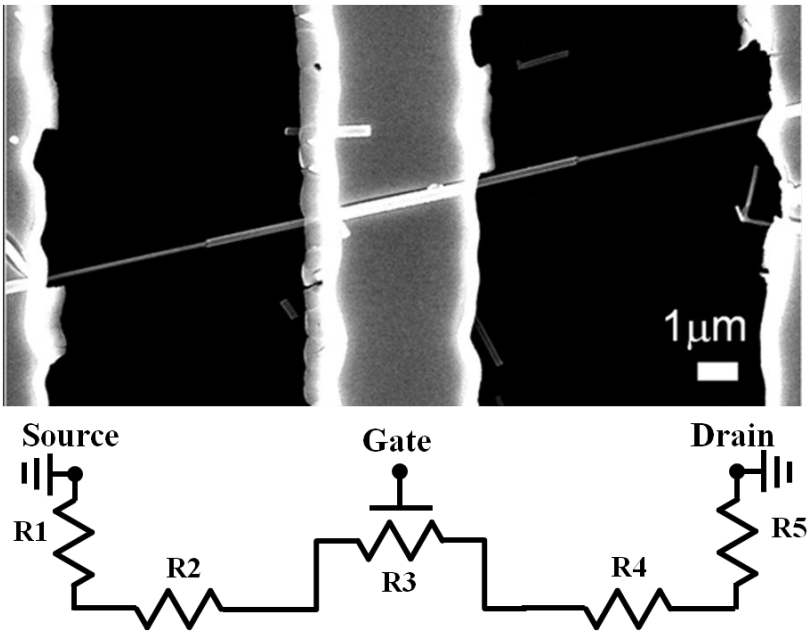

Fig. S6. SEM image of SiNWs GAA FET and schematics of equivalent dc circuit model for the SiNWs GAA FET. In order to extract the transconductance of SiNWs GAA FETs we established simple equivalent dc circuit model. Contact resistors (R_1 and R_5) and channel resistors (R_2 - R_4) are connected in series. Thus, $R_{total} = R_1 + R_2 + R_3 + R_4 + R_5$. Since the gate bias is locally applied to the channel, only the R_3, under the surrounding gate region, is critical variable. These resistance variations lead the current change because of the following equation: $I_{ds} = V_{ds}/R_{total}$ (V_{ds}=1V) Therefore, we can determine the transconductance of SiNWs GAA FETs from the I_{ds}-V_g curves in Fig. 5(b) without any consideration of contact resistance between NWs and metal electrode.