Supporting Information

Inorganic Proton Conducting Electrolyte Coupled Oxide-Based Dendritic Transistors for Synaptic Electronics

Chang J Wan[1,2)], Li Q Zhu[2)], Ju M Zhou[2)], Yi Shi[1)], Qing Wan[1,2 *)]

1) Nanjing University, School of Electronic Science & Engineering, Nanjing 210093, Jiangsu, Peoples Republic of China

2) Ningbo Institute of Materials Technology and Engineering, Chinese Academy of Sciences, Ningbo 315201, People's Republic of China

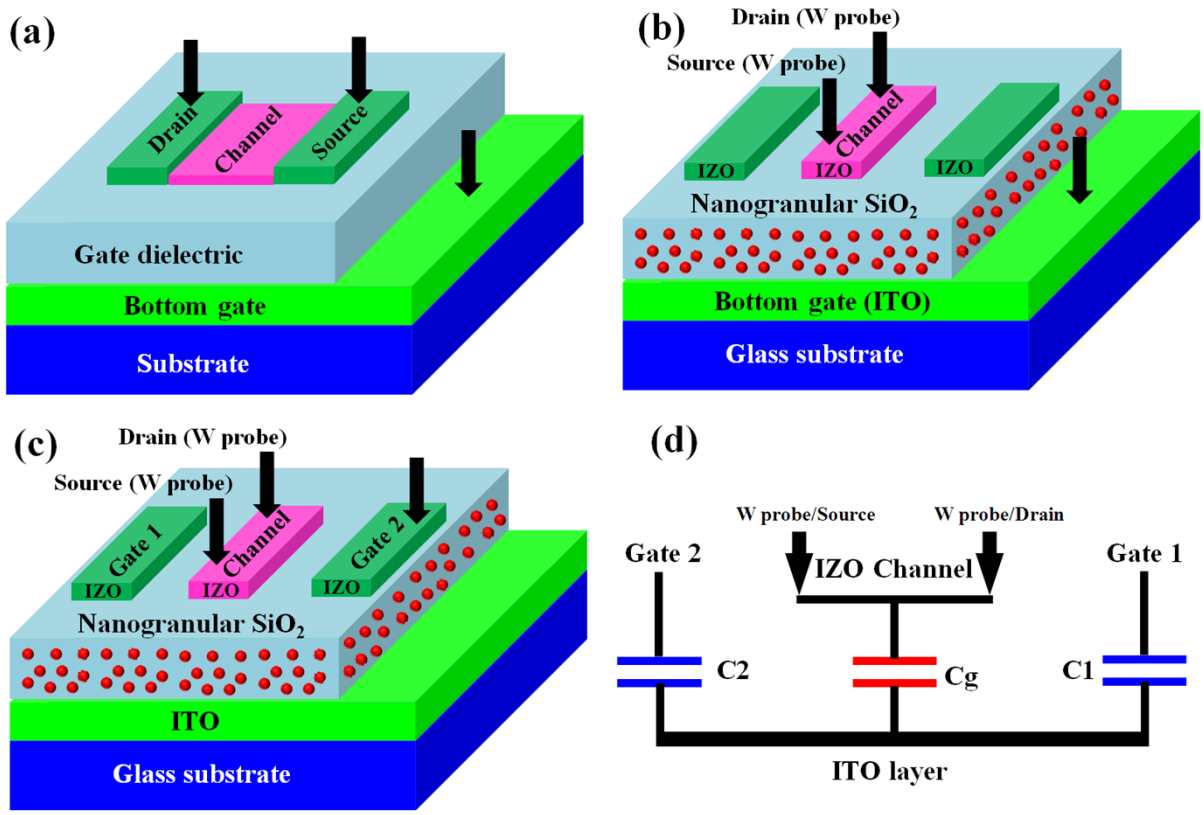

Figure S1. (a) Schematic image of a traditional transistor with bottom-gate structure. (b) IZO-based junctionless transistor with bottom-gate structure proposed in this work. (c) IZO-based junctionless transistor with in-plane gate structure proposed in this work. (d) Simplified circuit diagram for the dual in-plane gate IZO TFT. When positive bias is applied on G1 (or G2), two electric-double-layer capacitor would form at ITO/p-doped SiO_2 interface (C1/or C2) and p-doped SiO_2/IZO interface (Cg), respectively. The two capacitors are connected in series through the bottom conducting ITO layer.

Figure S1 (a) is the schematic image of a traditional transistor with bottom-gate structure. Source/drain electrodes are needed, and the gate coupling is realized vertically. In this work, the sputtered IZO films have a high carrier density in the order of $10^{19}/cm^3$ and a low resistivity of about 2×10^{-3} Ω·cm (measured by Hall measurements). Therefore a good ohmic contact would be addressed when contacting W probe to the patterned IZO film. When contacting two W probes to the patterned IZO film, the current on the IZO films could be obtained. Therefore, a junctionless transistor could be obtained. [1, 2] When the bottom ITO film

is used as gate electrode, a IZO junctionless transistor with bottom-gate structure is obtained, as shown in Figure S1 (b). No additional source and drain electrodes deposition is needed. The distance between the two W probes is ~300 μm (channel length). The gate voltage can be coupled to IZO channel due to the formation of electric-double-layer (EDL) at the interface of IZO/p-doped SiO_2. At the same time, the in-plane patterned IZO films could also be used as the in-plane gates (i.e. G1 and G2), as shown in Figure S1(c). When positive bias is applied on G1 (or G2), two electric-double-layer capacitors would form at ITO/p-doped SiO_2 interface (C1/or C2) and p-doped SiO_2/IZO interface (Cg), respectively. The two capacitors are connected in series through the bottom conducting ITO layer.

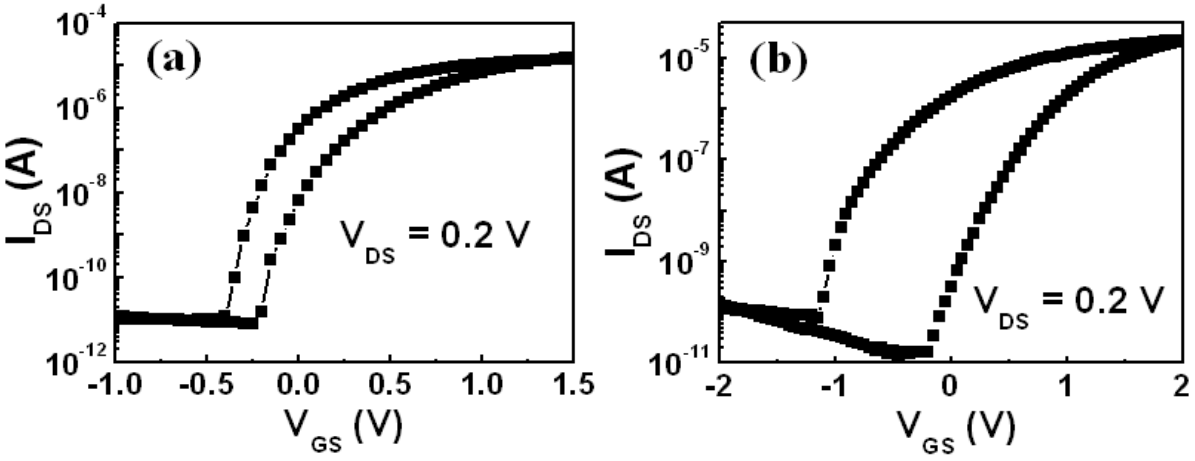

Figure S2 (a) Transfer curve of the IZO-based dendritic transistor measured by applying gate voltage on bottom gate with a constant V_{DS} of 0.2V. The inset shows the schematic diagram for the transistor with bottom gate structure. (b) Transfer curve of the IZO-based dendritic transistor measured by applying gate voltage on in-plane gate with a constant V_{DS} of 0.2V. The inset shows the schematic diagram for the transistor with in-plane gate structure.

Figure S2 (a) shows the transfer curve of the IZO-based dendritic transistor measured by applying gate voltage on bottom gate with a constant V_{DS} of 0.2V. The channel current on/off ratio is ~1.8×10^6 and the subthreshold slope is ~71 mV/decade. Figure S2 (b) shows the transfer curve of the IZO-based dendritic transistor measured by applying gate voltage on in-plane gate with a constant V_{DS} of 0.2 V. The current on/off ratio is ~2×10^6, the subthreshold

slope is ~163 mV/decade.

In the STDP emulations, the initial distribution profile of proton in nanogranualr SiO_2 electrolyte film is the equilibrium state, and protons are distributed uniformly in the nanogranualr SiO_2 electrolyte film. Yes, the middle-state weight control is crucial for the STDP experiments. As reported in our recent work, multilevel conductance state can be obtained by programing gate pulses. [3] If the channel conductance is higher (or lower) than the middle-state conductance, then negative (or positive) gate pulses were applied on the gate electrode. So a middle-state weight of ~0.1 μS with a relative deviation less than 5% can be obtained, as shown in FIG. S3.

When a pulse voltage was applied on the gate electrode (or IZO film) first, hydrogen bond in SiO_2 electrolyte and IZO would be broken up, and the ionized hydrogen would hopping yield the electric field. [4] Then, the ionized hydrogen would be drifted to the SiO_2 /ITO (or SiO_2/IZO) interface by the closely applied second pulse on IZO (or gate electrode). The hydrogen near the SiO_2/IZO interface would be depleted (or accumulated) by such processes, which lead a long term decrease (or increase) in IZO conductance. More residual ionized hydrogen would be obtained with closer pulse interval, which in turn leads more remarkable decrement (or increment) in conductance.

If the two pulses are separated with an enough long interval (e. g. few seconds), the net effect of the two pulses are nearly equivalent with two processes—the breaking of hydrogen bond and hopping between hydroxyl groups. If the two pulses are close enough, before the ionized hydrogen induced by the first pulse drift back to their equilibrium state, the second pulse would pull them back with less hydrogen bond breaking process. The schematic diagram of such processes are shown in FIG. S4. Thus the net effect is more decisive by the second pulse.

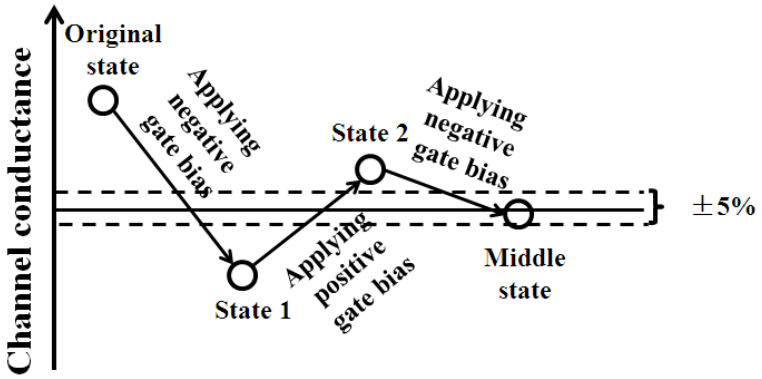

Figure. S3 Schematic diagram of the tuning strategies for obtaining of middle state conductance.

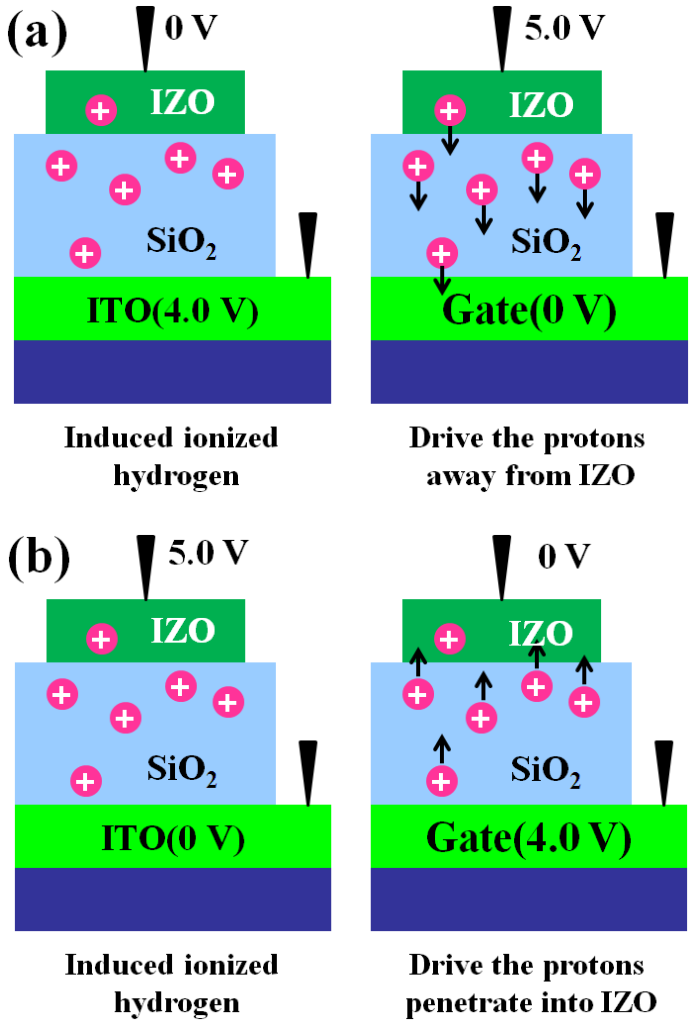

Figure. S4. The schematic diagram of the proton migration behaviors by the pair-spike. Spike applied on ITO gate first (a) and spike applied on IZO channel first (b).

Reference

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4. Zhu L. Q. et al. Self-assembled dual in-plane gate thin-film transistors gated by nanogranular SiO_2 proton conductors for logic applications Nanoscale, 5, 1980–1985 (2013)