Supplmentary Information for:

A Mechanical and Electrical Transistor Structure (METS) with a Sub-2 nm Nanogap for Effective Voltage Scaling

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1. The setup of the proper dielectric thickness to realize the smallest air gap

A proper thickness of the gate dielectric is required for a reduction of the pull-in voltage (V_P) with the aid of a nanoscale air gap. To realize this, it is necessary to find the accurate width of the initial air gap and the gap-fill ability (step coverage) of the deposited layer by atomic layer deposition (ALD). Figure S1 (A) shows a top-view scanning electron microscopy (SEM) image taken to identify the width of the initial air gap. Air gap widths of 15 nm were identified from a few SEM images, and HfO_2 of a thickness of 5 nm was deposited to reduce the air gap width to less than 5 nm. However, the V_P value did not change notably; hence, accurate analyses of the air gap and nanowire (NW) profile was indispensable. Figure S1 (B) shows a transmission electron microscopy (TEM) image captured to identify the accurate width of the air gap. As shown in Figure S1 (B), the actual width of the air gap from the TEM image was nearly twice that from the SEM image. This difference is attributed to the overhang profile of the gate and to the slope of the NW. In addition, the layer deposited by ALD shows outstanding step coverage and accurate thickness controllability even inside the nanoscale gap. With the aid of a TEM analysis, the proper deposition thickness of the dielectric was fixed to achieve a sub-2 nm air gap width.

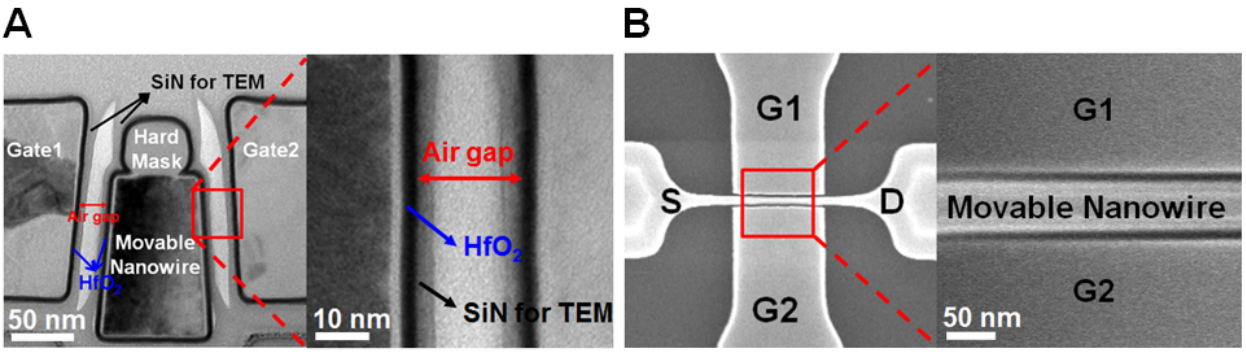

Figure S1. The SEM and TEM images analyzed for the accurate control of the air gap width. (A) A top-view SEM image of the fabricated METS. (B) A cross-sectional TEM image of the fabricated METS.

2. *X-ray photoelectron spectroscopy (XPS) data*

XPS data show the component elements incorporated in each gate dielectric. O, Al, and Hf are identified for the SiO_2, Al_2O_3, and HfO_2 samples, respectively. Thus, energy dispersive spectroscopy (EDS) mapping images to signify the elements in each dielectric are supported by the provided XPS data as shown in Figure S2.

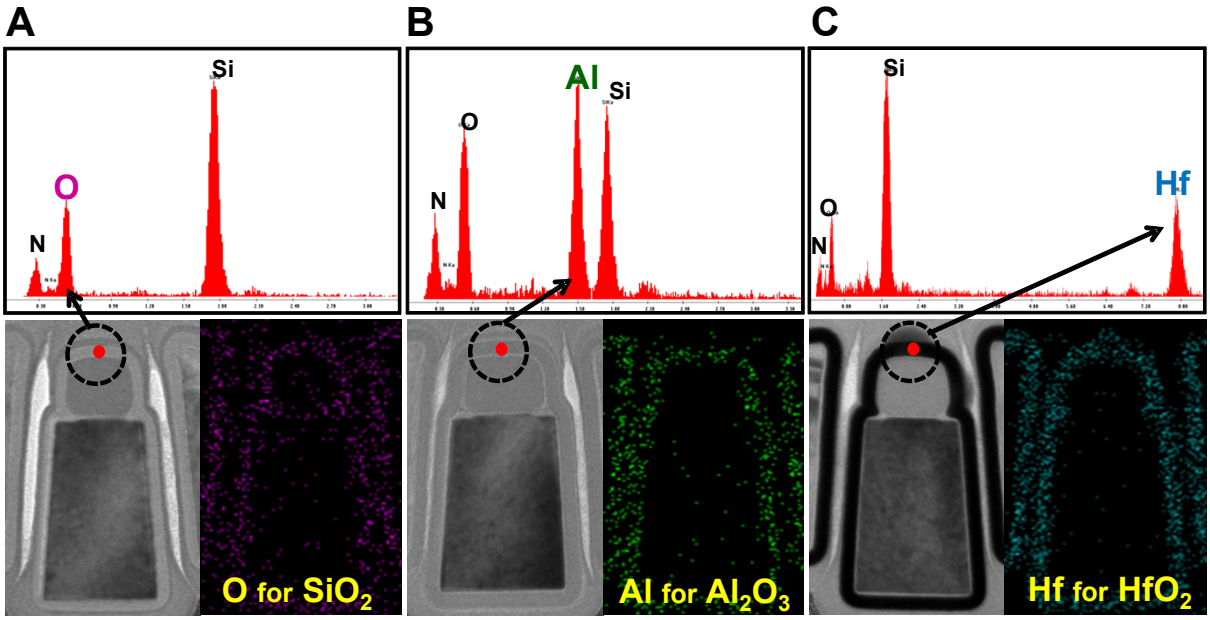

Figure S2. XPS data to analyze the component elements of each gate dielectric. The red point in the dashed black circle indicates the analyzed spot in each case. Cross-sectional TEM images and EDS mapping images of each dielectric are respectively included in (A), (B), and (C). (A) XPS data of O from SiO_2. (B) XPS data of Al from Al_2O_3. (C) XPS data of Hf from HfO_2

3. The simulation result for pull-in voltage of METS

In this study, a simulation using the finite element method (FEM) is applied to verify the experimental data. Figure S3 (A) shows the structure of the METS used for the simulation, which is represented by a fine mesh for the extraction of V_P. The physical parameters of this structure are identical to those of the experimental structure. Also, this structure is optimized such that it is closely matched to an actual structure observed in the SEM image; hence, good agreement is assured between the simulated and the experimental data. Crude and brief modeling is carried out, as shown in the following equation, to determine the value of V_P. Figure S3 (B) shows a brief schematic of the modeling:

$$F_{Spring} = k_{Spring} x, \qquad k_{Spring} = \frac{32 E_{Si} H_{NW} \left\{ \frac{W_{NW} + 2T_{Dielec}(E_{Dielec}/E_{Si})^{\frac{1}{3}}}{L_{NW}} \right\}^3}{8(\frac{l}{L_{NW}})^3 - 20(\frac{l}{L_{NW}})^2 + 14(\frac{l}{L_{NW}}) - 1},$$

$$F_{Electrostatic} = \frac{\varepsilon_0 A V_G^{\,2}}{2(W_{Air} + \frac{2T_{Dielec}}{k_{Dielec}} - x)^2}, \quad \text{and}$$

$$V_P = \sqrt{\frac{8k(W_{Air} + \frac{2T_{Dielec}}{k_{Dielec}})^3}{27\varepsilon_0 A}}.$$

Here k_{Spring} is the spring constant of the movable NW; E_{Si} and E_{Dielec} are the Young's modulus of the movable NW and the gate dielectric, respectively; H_{NW} is the height of NW; W_{Air}, T_{Dielec}, and W_{NW} are the width of the air gap, the thickness of the gate dielectric, and the width of the NW, respectively; k_{Dielec} is the dielectric constant of the gate dielectric; ε_0 is the permittivity of

vacuum; x denotes the displacement of the NW under the pull-in operation; and V_G is the applied gate bias. L_{NW} and l are the total length of the NW and the average values (=[L+L_G]/2) of L_G and L, as shown in Figure S3 (B). A is defined as the effective area, $h(2l - L_{NW})$. V_P is extracted from the condition in which F_{Spring} is equal to $F_{Electrostatic}$.

Figure S3 (C) shows the tunable V_P for the gate length (L_G) and the nanowire width (W_{NW}). The values of V_P are compared between the simulation and the analytical modeling for various L_G, W_{NW}, and gate dielectric conditions. They are crudely matched. Some discrepancies are attributed to the fact that the mesh structure is not identical to the fabricated structure and the fact that the proposed models are much too simplified for comprehensive modeling.

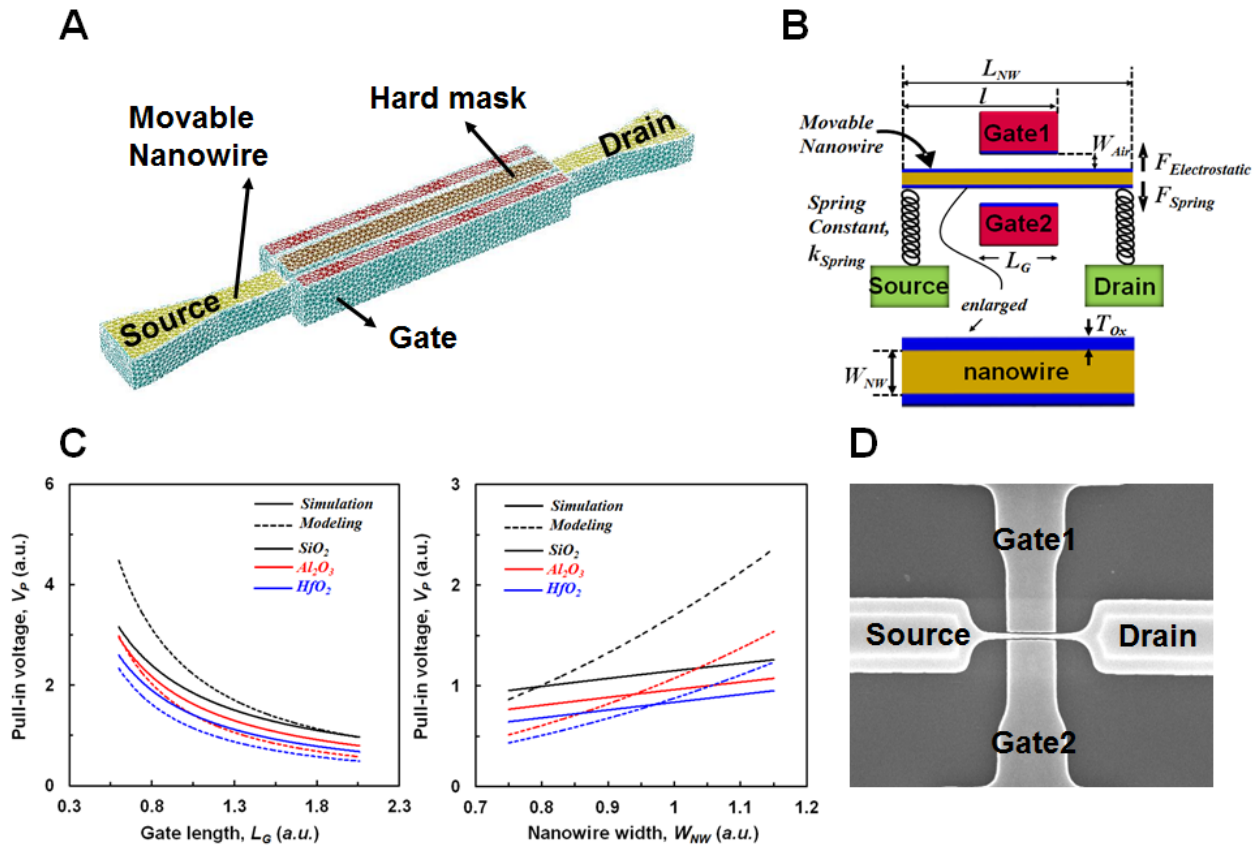

Figure S3. Figures related to the simulation and the analytical modeling. (A) The meshed structure of the METS for the FEM simulation. (B) A schematic of the analytical modeling used to extract V_P. (C) The geometric dependencies of V_P extracted from the numerical simulation and the analytical modeling. (D) Top-view SEM image of the METS.

4. The widened dimension margin in designing the NEMS-based switch in this study using METS

The proposed METS reduces V_P through the application of high-k dielectrics and the stable formation of the nanogap by the ALD. Thus, it provides a greater degree of freedom when designing the NEMS-based switch for application to various fields in terms of dimension controllability. Figure S4 (A) shows the V_P-L_G characteristic of different METS types with several dielectrics, as identified in the FEM simulation. As shown in Figure S4 (A), V_P increases when L_G is decreased, as expected, which is consistent with the tendency shown in the analytical equations related to V_P in the NEMS. Thus, the rapid increase of V_P due to the decreased L_G inhibits the further scaling of the NEMS device, including the METS. However, the application of a gate dielectric with a higher dielectric constant than SiO_2 allows for the scaling down of L_G, satisfying the same V_P, as shown in Figure S4 (B). The application of HfO_2, *i.e.*, replacing SiO_2 with HfO_2 to obtain a target V_P of 2 V, can realize the-scale down effect of L_G to about 30 %. With the same V_P value, Al_2O_3 showed a scale-down effect of about 13 %, lower than that of HfO_2. The target V_P can be modulated through the simple scaling of the METS.

Figure S4 (C) presents the FEM simulation result, which shows the dependency of V_P on the W_{NW} of the METS with each gate dielectric. As shown in Figure S4 (C), V_P is decreased with a decreased in W_{NW}, which is also consistent with the tendency shown in the analytical equations related to V_P in the NEMS. However, an aggressive reduction of W_{NW} to lower V_P can cause mechanical reliability issues, such as the fracturing of the NW owing to fatigue by iterative pull-in operations. The solution to alleviate this issue is shown in Figure S4 (D). Figure S4 (D) shows that the application of a higher dielectric constant than that of SiO_2, *i.e.*, the application of HfO_2 or Al_2O_3, allows for an increase of W_{NW} to obtain the target V_P. In order to meet the target V_P,

e.g., 2 V in this case, the W_{NW} value with the HfO_2 gate dielectric is widened by approximately 33 % more compared to that with the SiO_2 gate, which can contribute to improving the mechanical reliability. As expected, this is considered to result from the fact that the electrostatic force increased by the high-k reduces V_P and thereby provides an increased design margin in the physical dimensions of the NEMS-based switch including the METS, for application to various fields.

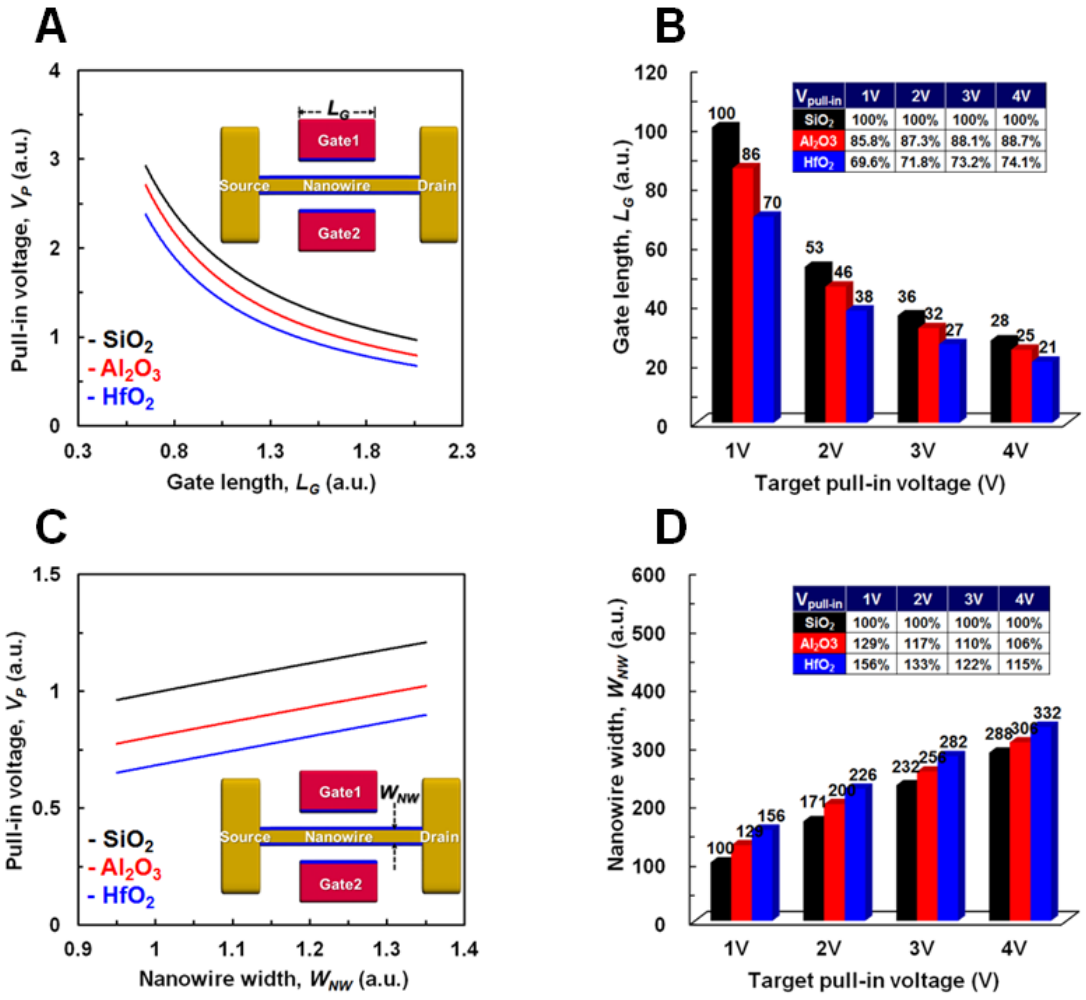

Figure S4. The geometric dependency of V_P. (A) V_P versus L_G characteristic for each gate dielectric. V_P is rapidly increased with a decrease in L_G, which is consistent with the tendency shown in the analytical equations related to V_P in the NEMS. (B) The required L_G to obtain the

targeted value of V_P. The table in the inset shows the relative percent ratio of L_G at SiO_2 to L_G with high-k dielectrics to satisfy the same targeted V_P. In order to satisfy the V_P of 2 V, the L_G value of the Al_2O_3 device and that of the HfO_2 device are roughly decreased by 13 % and 30 %, respectively, compared to the SiO_2 case. (C) V_P versus the W_{NW} characteristic for each gate dielectric. V_P is increased with an increase in W_{NW}, which is also consistent with the tendency shown in the analytical equations related to V_P in the NEMS. (D) The required W_{NW} to attain the target V_P. The table in the inset shows the relative percent ratio of W_{NW} at SiO_2 to W_{NW} with high-k dielectrics to satisfy the same targeted V_P. In order to meet V_P of 2 V, the W_{NW} value of the Al_2O_3 device and that of the HfO_2 device are increased roughly by 17 % and 33 %, respectively, compared to this value the SiO_2 device.

5. The introduction of the main parameters of the representative MEM, NEM switches

The characteristic parameters of representative micro-electro-mechanical (MEM) and nano-electro-mechanical (NEM) switch including pull-in voltage were well summarized in Table 1 of ref. [1]. For the sake of the convenience, the trend of pull-in voltage is shown in Figure S5 as a descending order of the pull-in voltage from the relevant references. Most of NEM switches have shown high pull-in voltages above 10 V owing to the operation principle relying on electrostatic force. But, it can be reduced below 1 V due to an extremely narrowed width of air gap[17], which was arisen from novel processes.

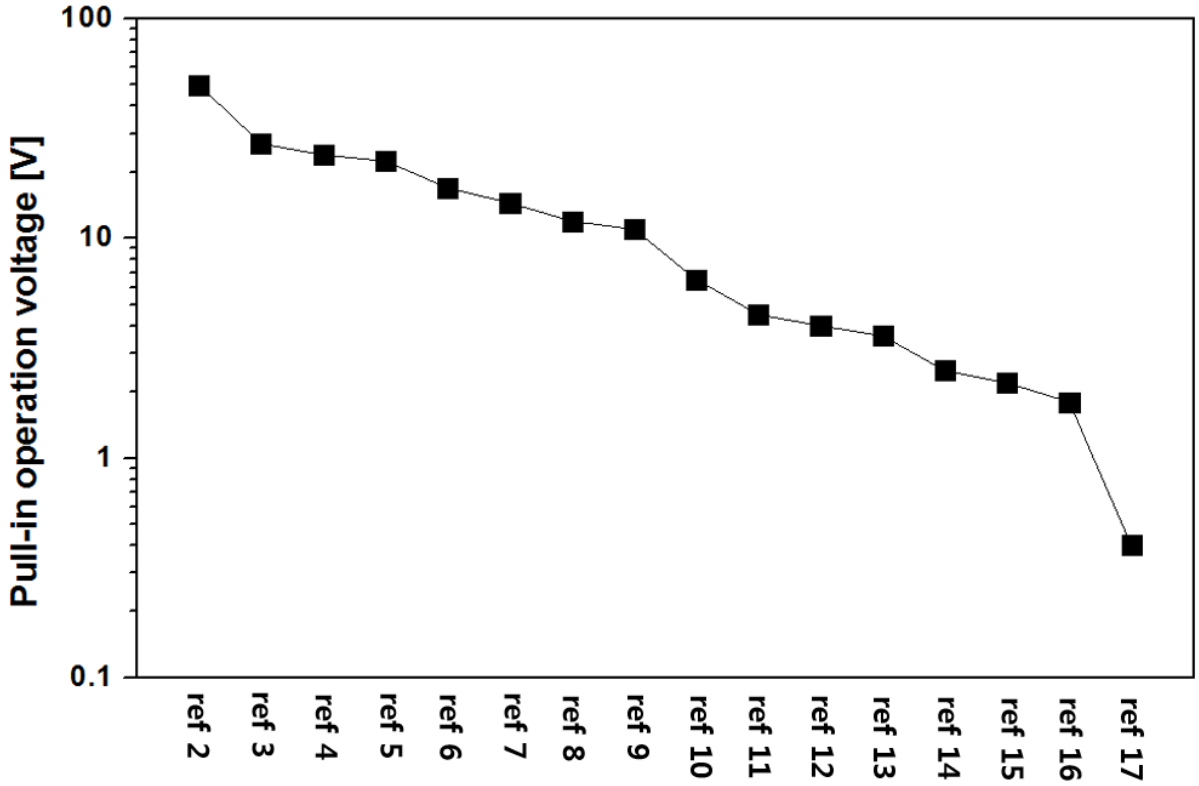

Figure S5. Trend of pull-in voltage

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6. *The explanation regarding Casmir effect and the strong immunity of METS against Casimir effect*

The stiction, which is a common failure of MEM and NEM switch, is caused by the attraction force between two materials. The force tends to increases as the air gap decreases thus it brings about the stiction failure. The undesired attraction force can be explained as Casimir force in terms of quantum theory. Casimir force is defined as the attraction force due to quantum vacuum fluctuation caused by the difference of energy density of electromagnetic field. It is known that the Casimir force is the most famous mechanical effect of vacuum fluctuation. According to quantum mechanics, the electromagnetic field has a fluctuation even though it is in a vacuum state, which strongly depends on the geometry of a given space. In order to help further understanding, two conducting plates with a vacuum space are assumed to be placed like figure below. One plate is fixed, while the other plate is movable. This structure is similar to a cantilever typed NEM switch. Since the energy density of electromagnetic field in the inside of the plates is different from that in the outside, the movable plate is subject to this difference even without any external force. The fluctuation exerts different forces between the inside and outside, which eventually makes movable plate move to the fixed plate. This is known as Casimir force, which causes the stiction failure.

As shown in the below figure, if another fixed plate is located to the same distance from the movable plate (the geometry of both sides of the movable plate is identical), both sides of movable plates, i.e., inside 1 and inside 2, can theoretically have the same energy density of the electromagnetic field. Thus, the movable plate can avoid the unwanted movement through the same quantum vacuum fluctuation of both sides, which can contribute to avoiding the stiction failure.

The suggested structure for this study has a symmetric structure that two gate electrodes are located to both sides of the movable nanowire unlike conventional MEM or NEM switch based on an asymmetric cantilever typed structure. Thus the proposed structure warrants the strong immunity against Casimir force inducing stiction fail.[1]

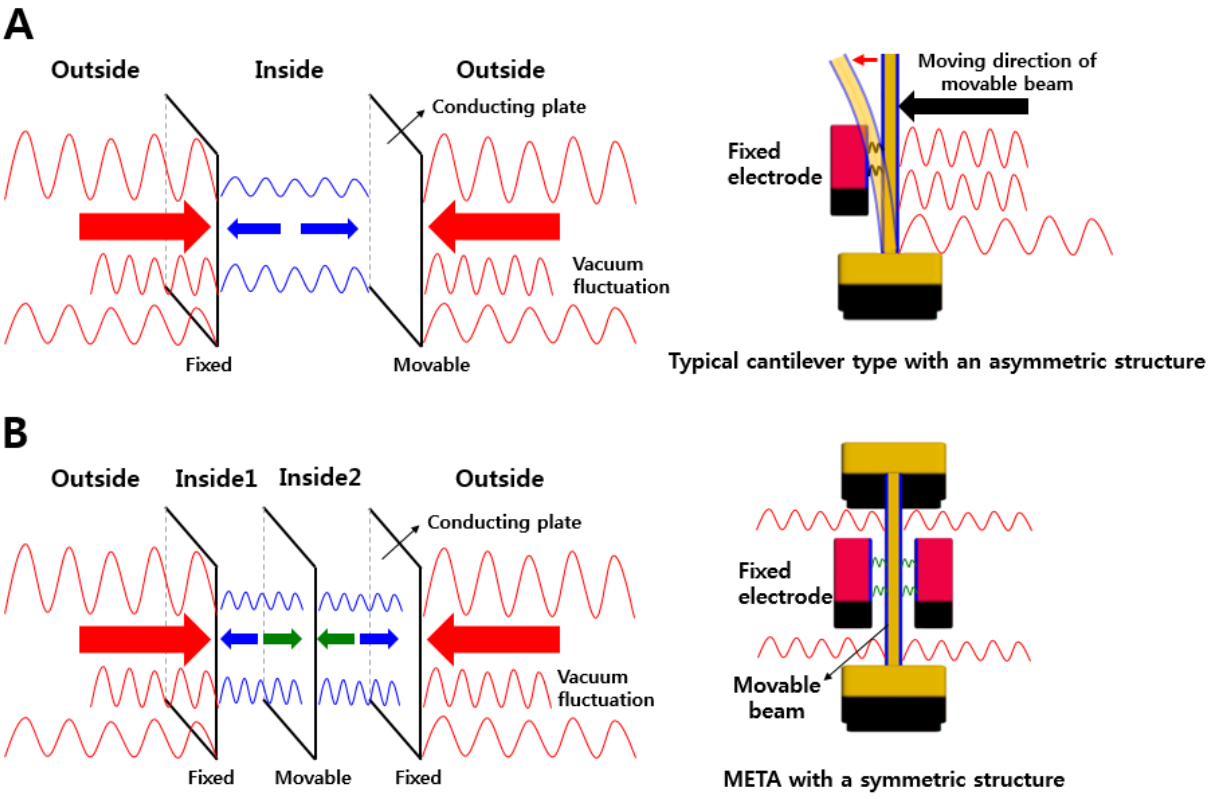

Figure S6. The effect of Casmir force under the different geometry. (A) The case of an asymmetric structure. (B) The case of a symmetric structure

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7. The comparison between typical method and the method for this study to build a nano gap

The air gap of a typical MEM and NEM switch is ordinarily built via the process as 1st method of below figure. The sacrificial layer between two conductors is deposited, and then removed by etch process. Since the sacrificial layer was usually removed by a wet etch process using wet etchant to circumvent problems such as physical damage of surface and unwanted residues, which are arisen from dry etch process. But, the aforementioned wet etch leads to causing the stiction failure, which becomes more severe as the air gap width, i.e., the thickness of sacrificial layer tends to decreases. Thus, the stiction problem impedes the building an ultra-narrow air gap below 10nm. This method is the 1st gap formation method mentioned in the manuscript.

The method for this study, *i.e.*, a 2nd method is to build an air gap using deposition of the suitable material such as dielectric or metal after the removal of a sacrificial layer. In order to form an air gap with the same width made by the 1st method, the 2nd method permits the thicker sacrificial layer than that of 1st method due to the following deposition process. Thus, the more widened air gap immediately after the removal of sacrificial layer can have a strong immunity against the stiction failure, compared to the 1st method. In this study, the air gap after removing sacrificial layer is precisely controlled by the application of ALD process. It is well known that ALD is the upmost deposition technology with numerous advantages, including accurate control of the thickness and excellent step coverage even in an extremely narrow gap, which allowed an

ultra-narrow air gap of sub-2 nm without the stiction in this study. This is the difference between two methods to build an air gap to have the same width.

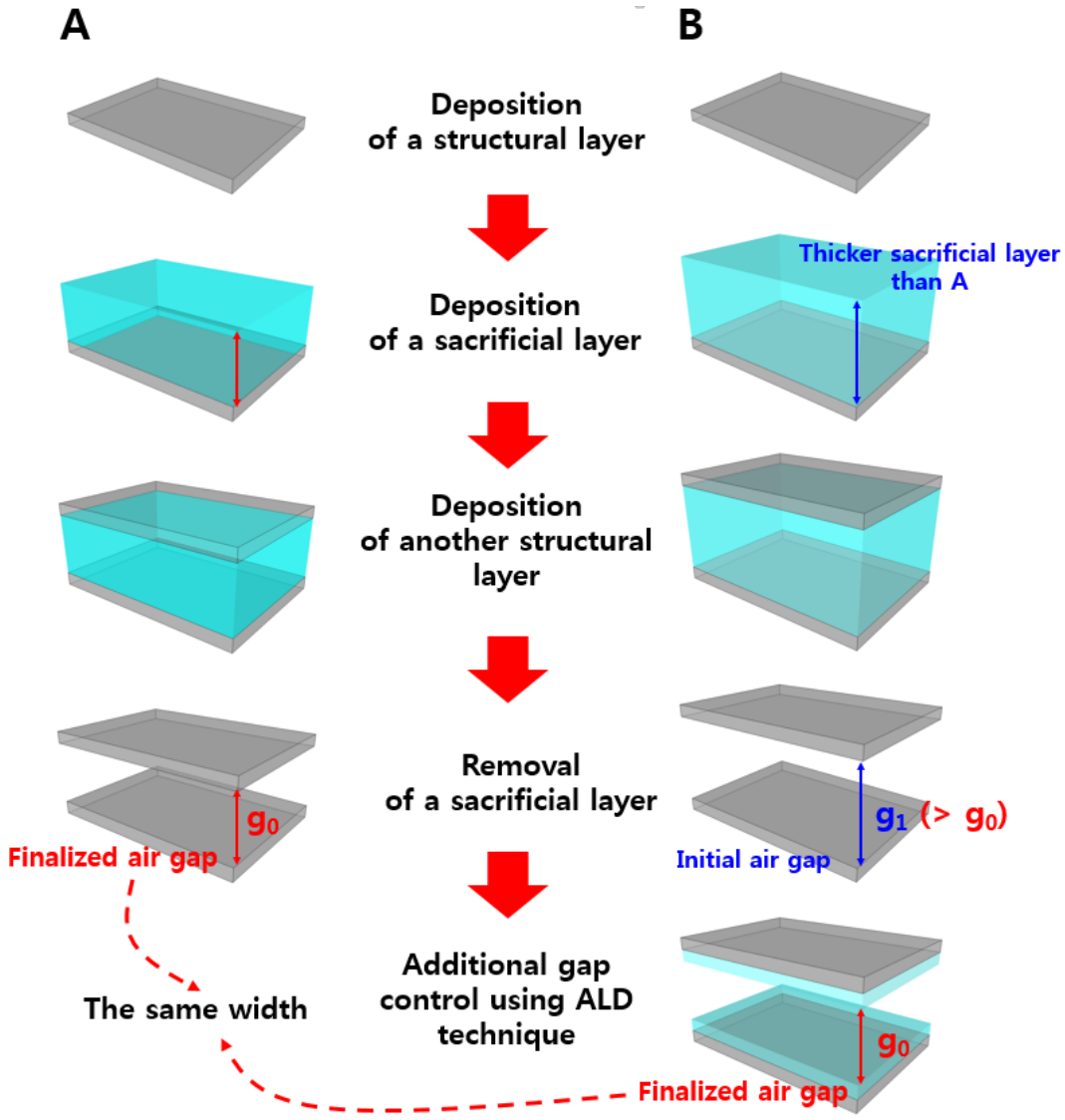


Figure S7. The methods to build the nano gap in the field of MEMS, NEMS based switch (A) Typical method, *i.e.*, 1st method (B) The method suggested for this study using ALD process, *i.e.*, 2nd method. This method permits the strong immunity against stiction fail during nano gap fabrication process

8. The modeling of pull-in, pull-out voltage for METS

In order to verify the theoretical feasibility of the operation, we conducted the modeling of pull-in and pull-out of METS. The modeling sequence is as follows:

Initially, the gate voltages can be expressed as the sum of the flat band voltage, voltage drop across the gate dielectric, and the semiconductor surface potential:

$$V_{g1} = V_{fb1} + V_{gox1} + V_{air1} + V_{fox1} + \phi_{s1} = V_{fb1} + V_1 + \phi_{s1}, \qquad (1)$$

$$V_{g2} = V_{fb2} + V_{gox2} + V_{air2} + V_{fox2} + \phi_{s2} = V_{fb2} + V_2 + \phi_{s2} \qquad (2)$$

where

V_{fb} : *flatband voltage*
V_{gox} : *voltage drop across gate oxide*
V_{air} : *voltage drop across air gap*
V_{fox} : *voltage drop across nanowire oxide*
ϕ_s : *surface potential*.

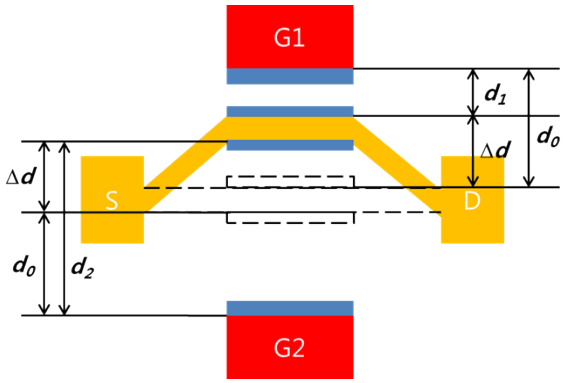
Here, the sub-indices 1 and 2 represent the front gate and back gate, respectively.
We then started the modeling process within the force-balance equation approximated as:

$$\frac{\varepsilon_{air} L_{gate} H V_2^2}{2 d_2^{\,2}} + k\Delta d = \frac{\varepsilon_{air} L_{gate} H V_1^2}{2 d_1^{\,2}} + F_a \qquad (3)$$

where

ε_{air} : *permittivity of air*
L_{gate} : *gate length*
H : *fin height*
k : *spring constant of the fin*
F_a : *surface adhesion force.*

The first term on the left and first term on the right represent the electrostatic forces applied to the back and front surface of the nanowire, respectively. $k\Delta d$ is the elastic restoring force of the nanowire and F_a is the surface adhesion force. In equation (3), k is the spring constant of the nanowire. The displacement of the nanowire Δd is $\Delta d=d_0-d_1$, where d_0 is the initial effective air gap thickness. d_1 is the equivalent air gap thickness between the front gate and the nanowire, and d_2 is the equivalent air gap thickness between the back gate and the nanowire. Following figure describes those parameters just mentioned above.



V_1 and V_2 can be obtained from the surface charges in channels Q_{s1} and Q_{s2}:

$$V_1 = -\frac{d_1 Q_{s1}}{\varepsilon_{air}}, \tag{4}$$

$$V_2 = -\frac{d_2 Q_{s2}}{\varepsilon_{air}}. \tag{5}$$

The adhesion force F_a is expressed as:

$$F_a = 2L_{gate} H \frac{\Gamma}{D_0} \tag{6}$$

where Γ is the adhesion energy per unit area and D_0 is the average distance between the two surfaces.[1] Using the above equations, we could derive the pull-in and pull-out model for the METS.

A. Pull-in State ($V_{g1}=V_{pi}$, $V_{g2}=0$)

Firstly, we tried to obtain the pull-in voltage since the operation of the METS starts with the pull-in state. The adhesion force term in (3) was ignored because the air gap thickness between two oxides is large before the pull-in occurs. The electrostatic force from the back gate was not considered in the pull-in voltage derivation since the back gate voltage is floated during the pull-in operation. Therefore, the force balance equation becomes simplified as:

$$k\Delta d = \frac{\varepsilon_{air} L_{gate} H V_1^2}{2 d_1^2}. \tag{7}$$

Herein, Δd can be obtained by substituting equation (4) into equation (7):

$$\Delta d = \frac{L_{gate} H}{2\varepsilon_{air} k} Q_{s1}^2. \tag{8}$$

Using the depletion approximation, the surface charges in the channel (Q_{s1}) can be expressed as a function of the surface potential as:

$$Q_{s1} = -\sqrt{2\varepsilon_{si} q N_A \phi_{s1}}. \tag{9}$$

By substituting equation (9) into equation (8), the displacement of the nanowire is finally expressed as a function of the surface potential:

$$\Delta d = \frac{\varepsilon_{si} q L_{gate} H N_A}{\varepsilon_{air} k} \phi_{s1}. \tag{10}$$

The gap distance between the front gate and the front channel in the pull-in mode is expressed as Ref.2:

$$d_{1,pi} = \frac{2 - C_{gap0} / C_{f1,pi}}{3} d_0 \tag{11}$$

where

$C_{f1,pi}$: *large signal capacitance in the front channel at the pull – in position*

C_{gap0} : *capacitance of the effective air gap including the gate oxide, air gap, and nanowire oxide at the front gate side* $(=\frac{\varepsilon_{air}}{d_0})$.

From equations (10) and (11), $C_{f1,pi}$ is derived as a function of the surface potential of the front gate channel by:

$$C_{f1,pi} = \frac{\varepsilon_{air}}{\frac{3\varepsilon_{si} q L_{gate} H N_A}{\varepsilon_{air} k} \phi_{s1,pi} - d_0}. \tag{12}$$

Given that the nanowire is in a weak inversion mode, C_{f1} is expressed as the ratio of the depletion charge to the surface potential in the front gate channel by:

$$C_{f1} = \left| \frac{Q_{s1}}{\phi_{s1}} \right| = \sqrt{\frac{2\varepsilon_{si} q N_A}{\phi_{s1}}}. \tag{13}$$

Pull-in will occur when the C_{f1} becomes $C_{f1,pi.}$ By equating equation (12) and (13), the front surface potential at the pull-in position is obtained by:

$$\phi_{pi} = \left(\frac{\beta + \sqrt{\beta^2 + 12\alpha d_0}}{6\alpha} \right)^2 \tag{14}$$

where

$$\alpha = \frac{\varepsilon_{si} q L_{gate} H N_A}{\varepsilon_{air} k}, \tag{15}$$

$$\beta = \frac{\varepsilon_{air}}{\sqrt{2\varepsilon_{air} q N_A}}. \tag{16}$$

Finally, the pull-in voltage is expressed as:

$$V_{pi} = V_{fb} + \frac{d_0 - \alpha\phi_{s1,pi}}{\beta} \sqrt{\phi_{s1,pi}} + \phi_{s1,pi}. \tag{17}$$

B. Pull-out State (V_{g1}=0, V_{g2}=V_{po})

The equivalent air gap thickness between the back gate and the nanowire (d_2) must be same with twice the initial effective air gap thickness (d_0) when the nanowire is pulled-in, whereas the equivalent air gap thickness between the front gate and the nanowire (d_1) becomes T_{gox}+T_{fox}. Herein, the T_{gox} and T_{fox} represent the thickness of the gate oxide and the nanowire oxide. In the pull-in state, the adhesion force cannot be ignored anymore since the nanowire is adhered to the front gate. Due to the work function difference, the electrostatic force between the front gate and the nanowire should be considered as well. Therefore, the force balance equation becomes:

$$\frac{\varepsilon_{air} L_{gate} H V_2^2}{2 d_2^{\,2}} + k\Delta d = \frac{\varepsilon_{air} L_{gate} H V_1^2}{2 d_1^{\,2}} + F_a . \tag{18}$$

V_1 and V_2 can be again obtained from the surface charges in channels Q_{s1} and Q_{s2}:

$$V_1 = -\frac{T_{ox} Q_{s1}}{\varepsilon_{ox}} = \frac{T_{ox}\sqrt{2qN_A\varepsilon_{si}\phi_{s1}}}{\varepsilon_{ox}}, \tag{19}$$

$$V_2 = -\frac{T_{ox} Q_{s2}}{\varepsilon_{ox}} = \frac{T_{ox}\sqrt{2qN_A\varepsilon_{si}\phi_{s2}}}{\varepsilon_{ox}}. \tag{20}$$

Substituting equation (19) into equation (1) yields the surface potential of the front gate, Φ_{s1}, can be obtained:

$$\phi_{s1} = \left(\frac{-\frac{T_{ox}\sqrt{2qN_A\varepsilon_{si}}}{\varepsilon_{ox}} + \sqrt{\frac{2qN_A\varepsilon_{si}T_{ox}^2}{\varepsilon_{ox}^2} - 4V_{fb}}}{2} \right)^2 . \tag{21}$$

The surface potential of the back gate, Φ_{s2}, can be attained by substituting equation (19), (20) and (21) into equation (18):

$$\phi_{s2,po} = \frac{\varepsilon_{air}}{\varepsilon_{ox}}\phi_{s1} + \frac{\varepsilon_{air}}{qN_A\varepsilon_{si}L_{gate}H}(F_a - kT_{air}). \tag{22}$$

Finally, the pull-out voltage is expressed as:

$$V_{po} = V_{fb} + \frac{2d_0\sqrt{2\varepsilon_{si}qN_A\phi_{s2,po}}}{\varepsilon_{air}} + \phi_{s1,po}. \quad (23)$$

Figure S8 (A), (B) show the surface potential according to the variation of gate voltage from 0V to 1V. It is clear that the surface potential is larger for the front gate voltage variation case in the initial state than the back gate voltage variation case in the pull-in state.

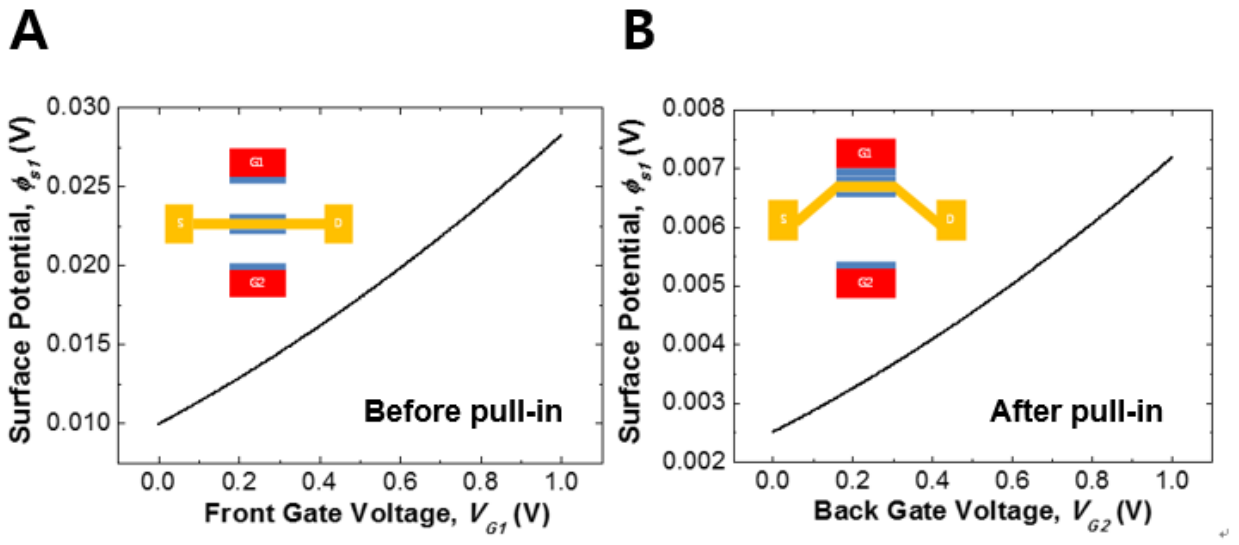


Figure S8 (A) The variation of surface potential by front gate voltage before pull-in. (B) The variation of surface potential by back gate voltage after pull-in

The Figure S8 (C) shows the variation of the pull-in and pull-out voltages with respect to air-gap thickness when L_{gate} = 300 nm, H = 100 nm, Na = 5x10^{18} cm^{-3}, L_{fin} = 600 nm, W = 20 nm, and T_{ox} = 4 nm. The variation of the pull-out voltage versus the air-gap thickness shows a noticeable trend. The pull-out voltage increases as the air-gap thickness increases until it meets a maximum value where the pull-out voltage starts to decrease again. Within the air-gap thicknesses less than the maximum value, the electrostatic force dominates the fin's movement

whereas the elastic restoring force cancels out the adhesion force, which means only a little electrostatic force is required at the back gate.

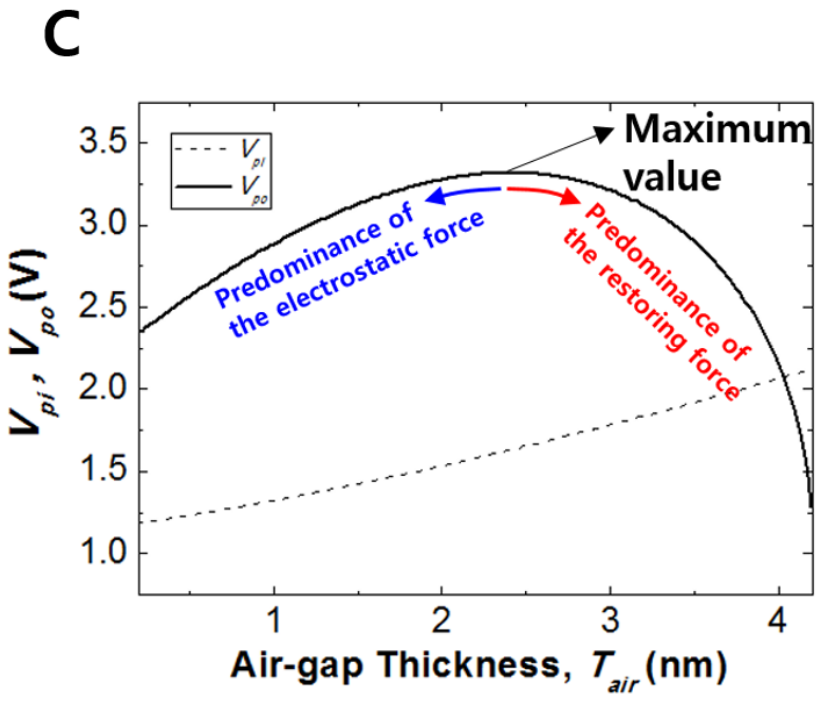


Figure S8 (C) The pull-in, pull-out voltage versus air gap. In addition to electrostatic force, the adhesion, restoring force is considered for the operation.

This modeling demonstrates that the control of nano gap using ALD, which is suggested by this study, is an effective method for operation voltage scaling. This modeling also shows that the physical optimization and proper surface treatment can allow a similar pull-in and pull-out voltage for METS, which demonstrates the feasibility of METS with low voltage for pull-in and pull-out.

Reference

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