Supporting Information

Density of States Limited Anomalous Current Saturation of Graphene Field Effect Transistors: Kinks and Negative Differential Resistances

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Calibration of HfO_x dielectrics

To accurately evaluate and model the gate modulation in GFET devices, the gate dielectric layer should be calibrated at first. We use *C-f* measurement to determine the gate capacitance as well as to detect the trap capacitance. Fig S1 illustrates the gold/HfO_x/Si plate capacitance with 500 μm by 500 μm pad area versus frequency, under different bias voltages. The total gate capacitance is extracted to be 0.7 μF/cm^2.The variation under different gate voltages is ascribed to trap states in the HfO_x surfaces. This variation is extremely large for positive gate voltages, therefore, to accurately model the device, we mainly use the negative gate voltage.

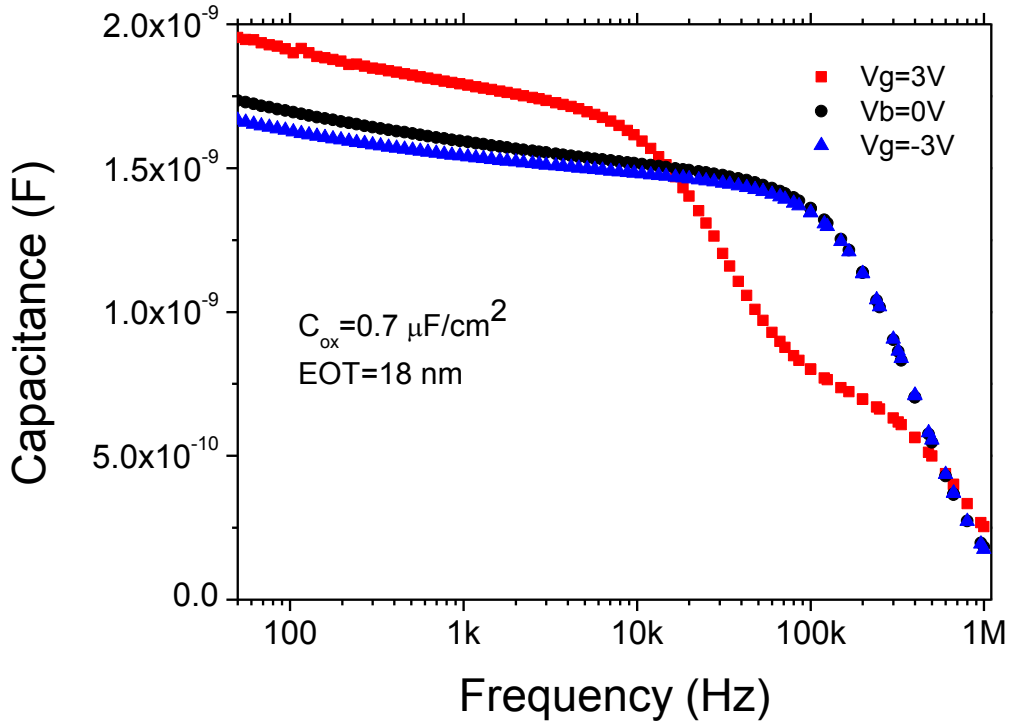
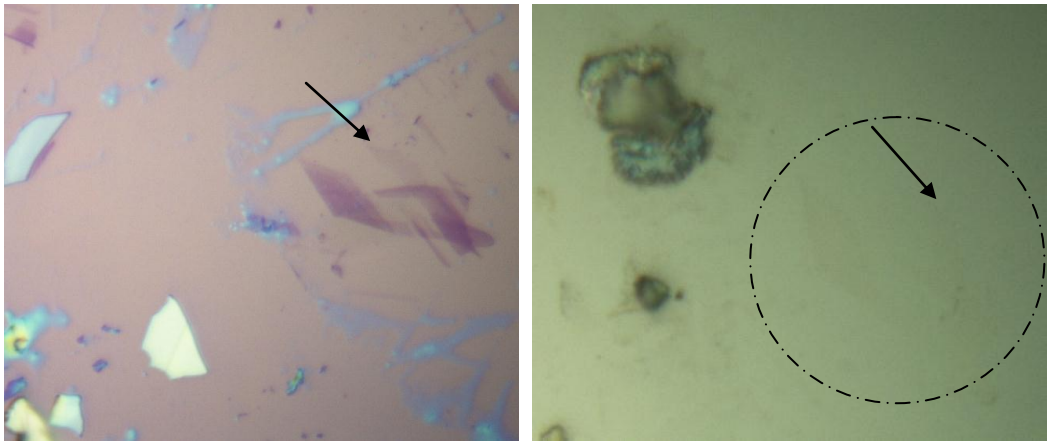


Fig. S1 Capacitance versus frequency of HfO_x dielectric under different biases

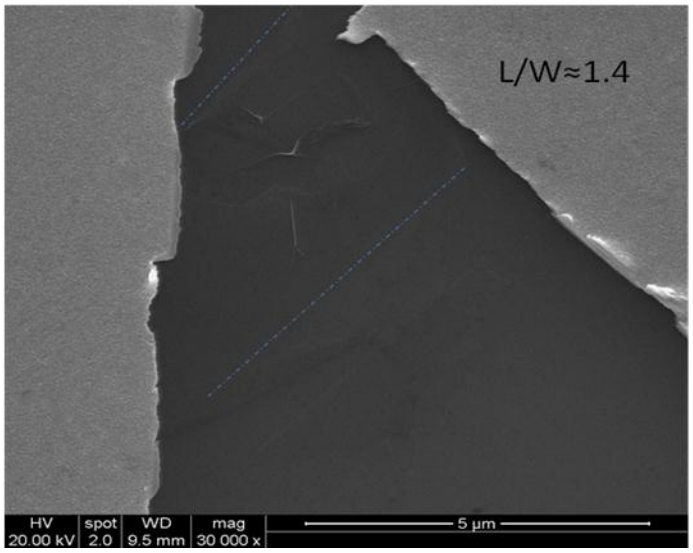
GFET fabrication

Due to optical contrast obtained on HfO_x substrate is unfavorable, it is extremely hard to identify graphene sheets and fabricate GFETs by directly transferring exfoliated graphene onto HfO_x substrate. Therefore, we used a two-step transfer process where mono-layer graphene was identified on SiO_2 and then transfer to HfO_x by means of deterministic placement. Few-layer graphene sheets were prepared and characterized on SiO_2 substrate at first. Mono-layer graphene was selected under optical microscopy and then identified by Raman spectrum, as shown in Fig S2

(a). Afterwards, a thin PMMA layer was spin coated (about 150 nm by 3000 rpm) above the SiO_2 surface. A small region (about 500 m by 500 m) was isolated by cutting with a micro-manipulator. The SiO_2 was then removed by soaking in hot KOH solution (1 mol/L 69 centidegree). The small piece of PMMA supporting film was reisined in DI water at first and then in an IPA bath. Finally, the PMMA film was deposited on HfO_x substrate and removed by warm Acetone (35 centidegree) for 1 hour. Fig S2 (b) shows the same graphene sample as in Fig S2 (a). Comparing to SiO_2 substrate, the optical contrast of mono-layer part is almost invisible on HfO dielectrics. The GFET after electrodes fabricated is shown in Fig S2 (c).



(a) (b)



(c)

Fig S2 Fabrication process of back-gate GFET on HfO_x substrate. (a) Few-layer graphene samples on Si wafer with 300 nm SiO_2 (b) The same sample after transfer to HfO_x substrate. The monolayer part is labeled by arrow. (c) SEM image of the device

KPFM Test

A Dimension 3100 AFM (Veeco) with a conductive tip operated in KPFM mode is used to acquire morphological and surface potential signals in a dual-pass scanning mode. The scanning starts with a topographic imaging line-scan in the tapping mode, a succeeding (interleave) pass retraces along the same scan line, where the tip is biased with a DC voltage V_{tip} and lifted at a fixed height above the surface. The electrostatic interaction caused by tip-sample capacitive coupling modulates the tapping frequency, altering both the phase and amplitude signals. By adjusting the applied V_{tip} to compensate the induced component, the surface potential information can be obtained. In the measurement, a lock-in amplifier is used to extract the capacitive force; under zero bias, the force could be described by

$$F(w) = - C(V_{tip} - V_0)U_{ac} \sin(wt)$$

where C is the spatial gradient of probe-sample capacitance, and V_0 is the contact potential difference (CPD) between the tip and sample, defined as $V_0 = (\Phi_{tip} - \Phi_{sample}) / q$. With an additional feedback loop, the CPD is mapped by nulling the induced force at the resonance frequency.

As in the KPFM configuration, parasitic capacitance including tip capacitance and the so-called quantum capacitance need to be considered. Fortunately, a detailed analysis shows that both of them are negligible, if the tip-sample capacitance is small, or equivalently, the lift height is large, e.g., as high as 10 nm. It is also worth to recall that due to the absolute CPD value is sensitive to variety environmental factors, the relative CPD between graphene and gold electrode which is invariant should be considered in the experiments. During all the tests, the humidity and temperature are kept at 85% and 295K, respectively. The sharp change of morphology in graphene/electrode contact region is another non-ideal factor which may limit the resolution of KPFM, which is marked as grey box in the KPFM test. Finally, due to under high filed bias, GFET is easy to breakdown; the KPFM measurements are carried out in a relatively high speed at cost of losing some spatial resolution, especially in the regions of that surface potential quickly changes. As a result, some artificial negative values of dV/dx may appear.

Obviously, under a certain bias, the CPD should be revised according to the local bias. Considering the region under test is locally biased to V, as illustrated in Fig S3. the equivalent

compensating voltage changes to V_{tip}-V instead of V_{tip} itself. Specific to our experimental configuration, the local bias voltage could be expressed by the local chemical potential.

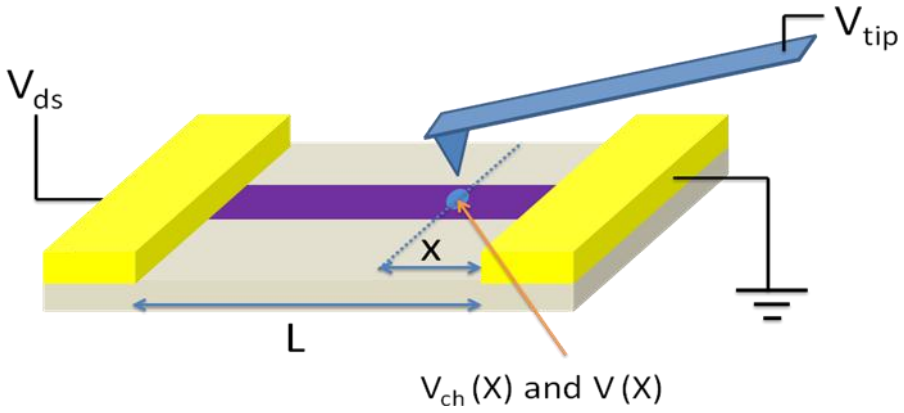


Fig S3 Schematic of the KPFM measurements

In this scenario, the CPD can be finally derived as:

$$V_{tip} - V(x) = (\Phi_{tip} - \Phi(x)) / q$$

$$\longrightarrow$$

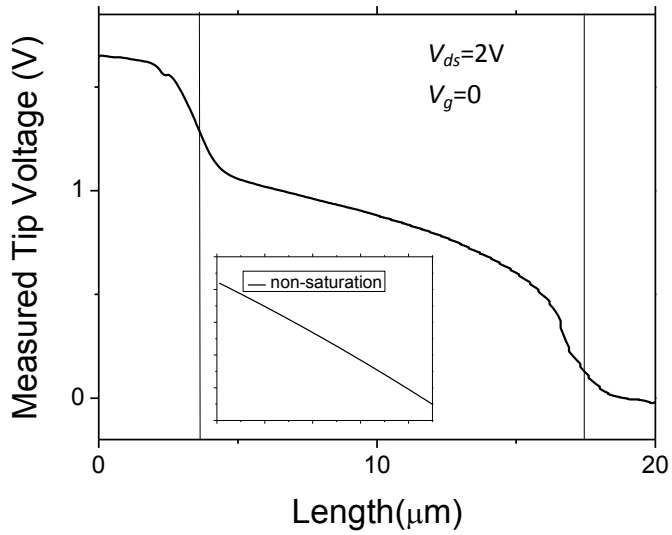
$$V_{tip} = V_{ch}(x) + V(x) - E_{f-tip} / q$$

$$\longrightarrow$$

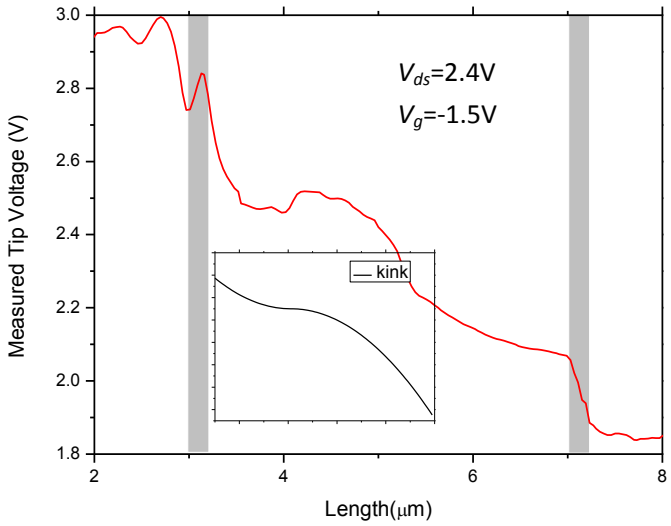
$$V_{tip} = V_g - \frac{\frac{1}{2}C_q}{C_{HfO}} V(x) - V_{f-tip}$$

$$= V_g - \frac{kV(x)|V(x)|}{2C_{HfO}} - V_{f-tip}$$

In addition to the NDR case that is demonstrated in the maintext, the KPFM could be also used to map the spatial potential distribution of non-saturation and kinks cases. Fig S4 (a) and (b) show the comparisons between simulation and measured tip voltage in non-saturation and kinks cases, respectively. The measured tip voltages qualitatively agree with the simulation, supporting our hypothesis on the carrier density distribution.



(a)



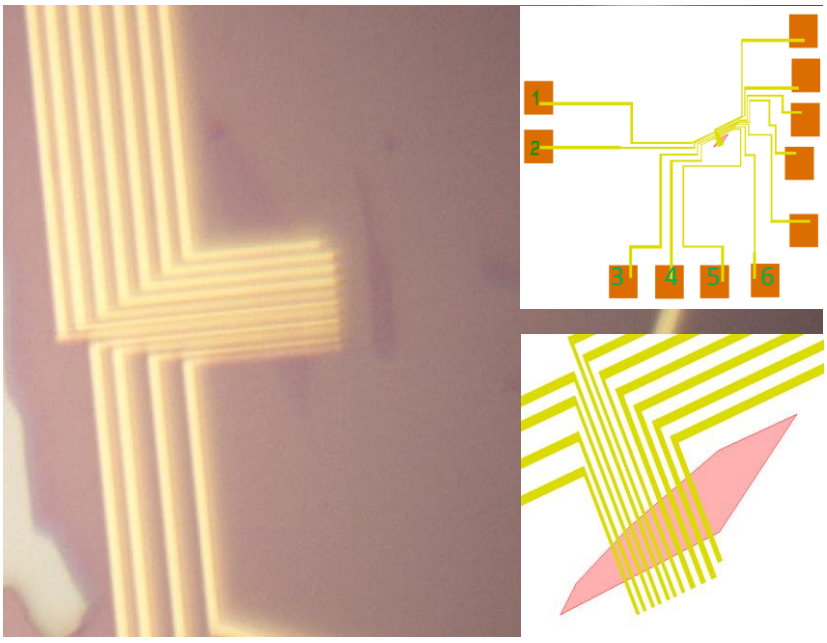
(b)

Fig S4 KPFM potential profiles of GFETs on HfO_x

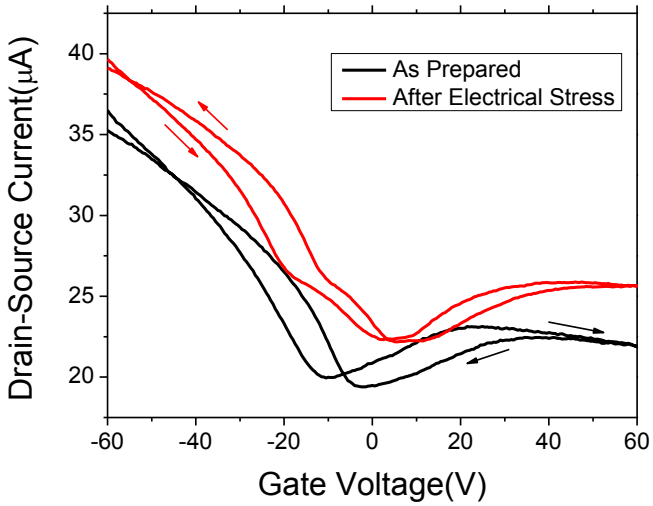
NDR of *p-n* junctions

The NDR effect could be also observed in GFET with *p-n* junction. In this case, the chemical doping creates sufficient increase of Fermi-level and may result in a broken of condition (3) even with a relatively small lateral electric field. To demonstrate this effect, we fabricated graphene FET with multiple electrodes on 300nm silica substrate by conventional E-beam lithography and lift-off process, as shown in Fig S5 (a). The transfer curve of as prepared device (electrode 2 as source and electrode 4 as drain) is as the black curve in Fig S5 (b) The output curve is plotted as in Fig S5 (c), the currents present non-saturation behavior up to 4 V bias voltages.

We then apply an electric stress form 0 to 7V between electrode 2 and 4. After that, as previously reported, under the gate doping, two dips appear in the I_{ds}-V_g curve as plotted in Fig S5 (b), corresponding to the p-part and n-part graphene flakes. Interestingly, under high field bias, the output curves exhibit obvious NDR effect, as shown in Fig S5 (d). This NDR effect could be understood by a same mechanism as stated in the maintext.



(a)



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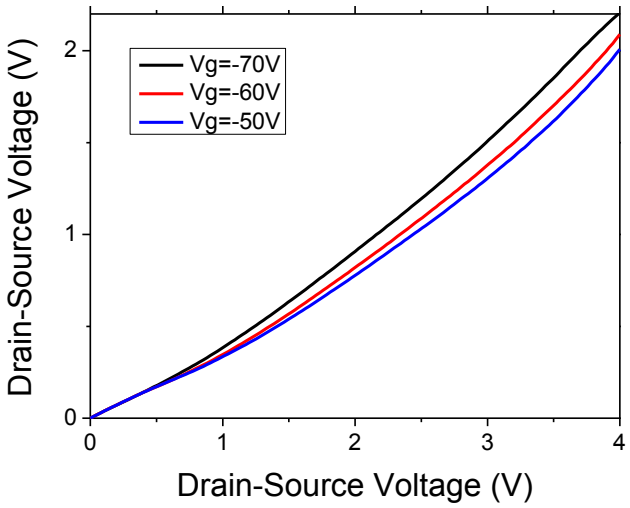
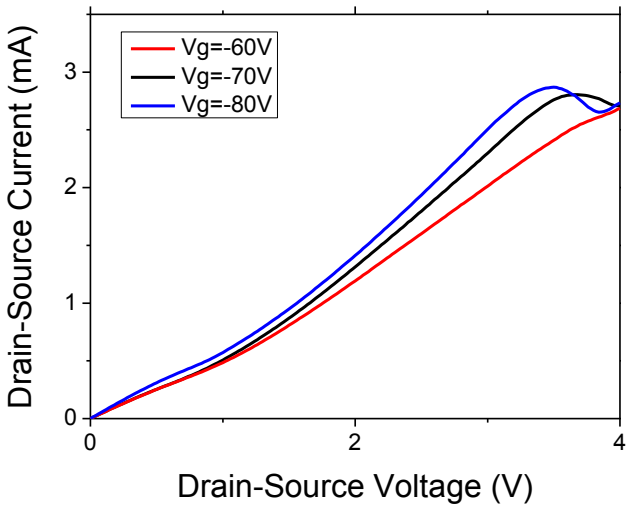
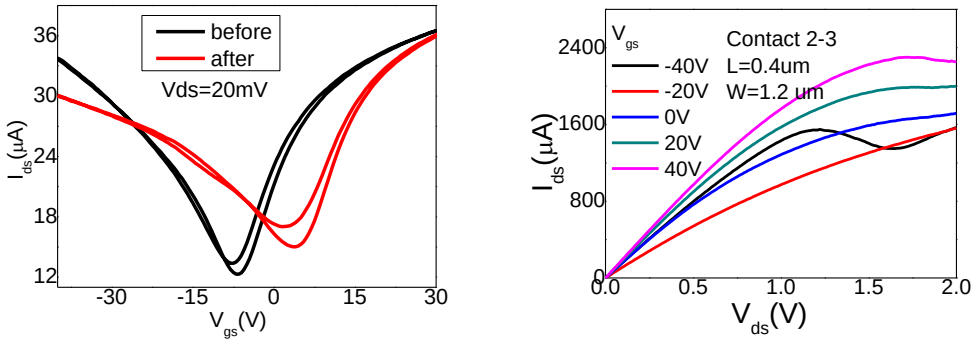


(c)



(d)

Fig S5 NDR in GFET on SiO_2/Si substrate (a) Images of the multi electrode devices (Inset) Top: the schematic of pad number. Bottom: the schematic of lead connection. (b) Transfer curves between 2 and 4: as-prepared device (black) and after electric stress applied (red) (c-d) Output curves between 2 and 4: as-prepared device (c) and after electric stress applied (d)



(a) (b)

Fig S6 NDR in GFET on SiO_2/Si substrate under vacuum conditions (a) Transfer curves of the GFET: as-prepared device (black) and after electric stress applied (red) (b) Output curves after electric stress applied

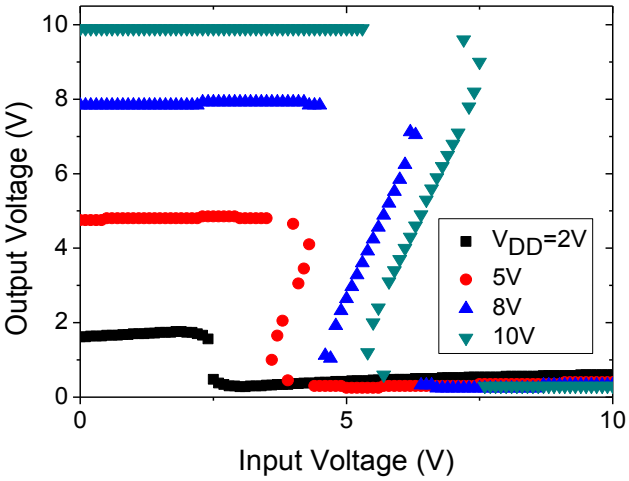
The Influence of NDR

1. Digital Applications

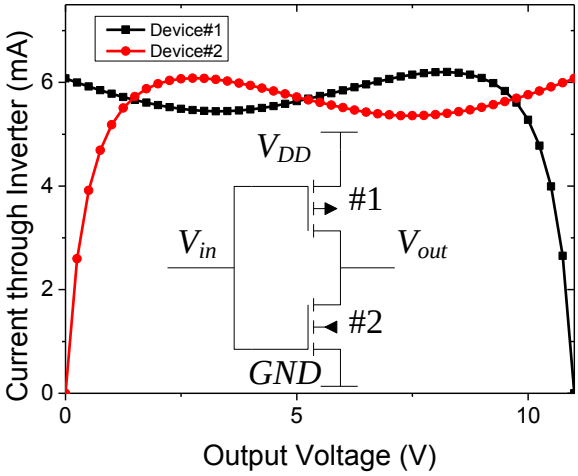
In the following sections, we move to discuss the influence of NDR to GFET applications. The fundamental graphene logic gates (NOT, NAND and NOR) operated in strong field region may yield further exotic behaviors than its counterpart biased in weak field [7, 26-27]. Similar as the treatment of contact resistances, inserting port voltages in each node and solving them from the current equation by load-line method, nodal voltages and branch circuits can be obtained. For instance, typical complementary NOT, NAND and NOR gates can be modeled as follows. As is illustrated in the Fig. S7 b, the NOT gate has two devices connected in series, the current through device #1 is equal to that through device #2. Treat V_{out} as unknown, one can easily derive the following equation

$$I_{ds1}(V_{in}, V_{B1}, V_{DD}, V_{out}) = I_{ds2}(V_{in}, V_{B2}, V_{out}, GND)$$

By solving this equation, one can finally obtain the numeric output characteristics of a NOT gate, as shown in Fig. S7 a. As we can see, the result shows the inverted characteristics. But when V_{DD} is increased, the curve starts to become "Z" like. This means that for a single V_{in}, there possibly exist multiple outputs. This effect can be simply understood by the multiple solutions of the current equation arise from the multiple intersection points for NDR devices as demonstrated in Fig. S7 b.



(a)

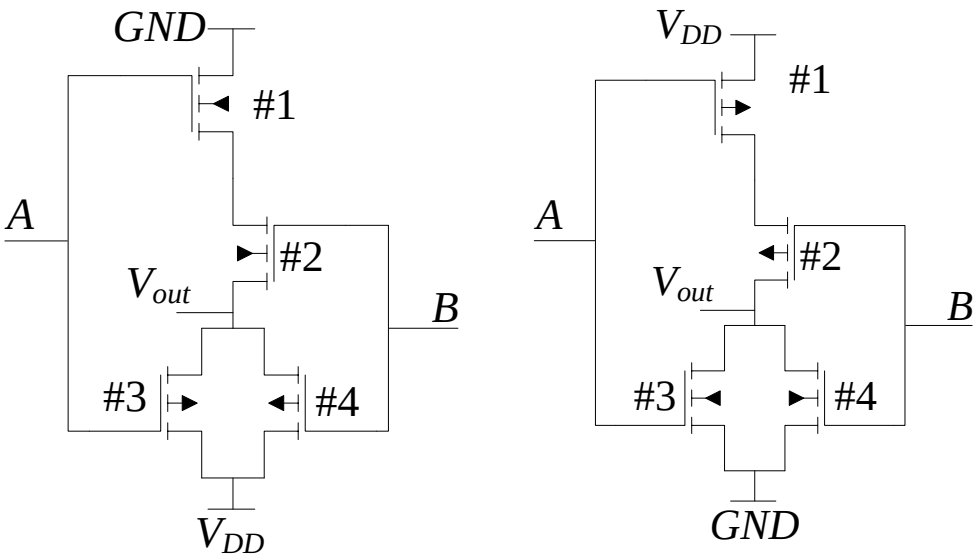


(b)

Fig S7. (a) Simulated output characteristics of graphene inverter under different bias conditions (b) Principle of multi-state effect. The two NDR devices yield multiple operation points. (Inset) Schematics of graphene inverter

There are even more multi-stable states for a NAND gate compared with those for a NOT gate. Figure S8 shows the schematic circuit diagram of a NAND and NOR gate. They are of the same structure except VDD and GND positions are reversed. In this case, we can also treat the V_{out} as the unknown and solve the equation set with two unknowns V_{out} and V_{temp}. Assuming the voltage between device #1 and device #2 is V_{temp}, and the upper terminal and the lower one are V_C and V_D respectively. The current equations read:

$$\begin{cases} I_{ds1}(A,V_{B1},V_C,V_{temp}) = I_{ds2}(B,V_{B2},V_{temp},V_{out}) \\ I_{ds2}(B,V_{B2},V_{temp},V_{out}) = I_{ds3}(A,V_{B3},V_{out},V_D) + I_{ds4}(B,V_{B3},V_{out},V_D) \end{cases}$$



(a) (b)

Figure S8 Schematics of (a) NAND and (b) NOR gates

Despite the low ON/OFF ratio, the truth-table-like graphs in Fig S9 illustrate standard NAND and NOR characteristics.

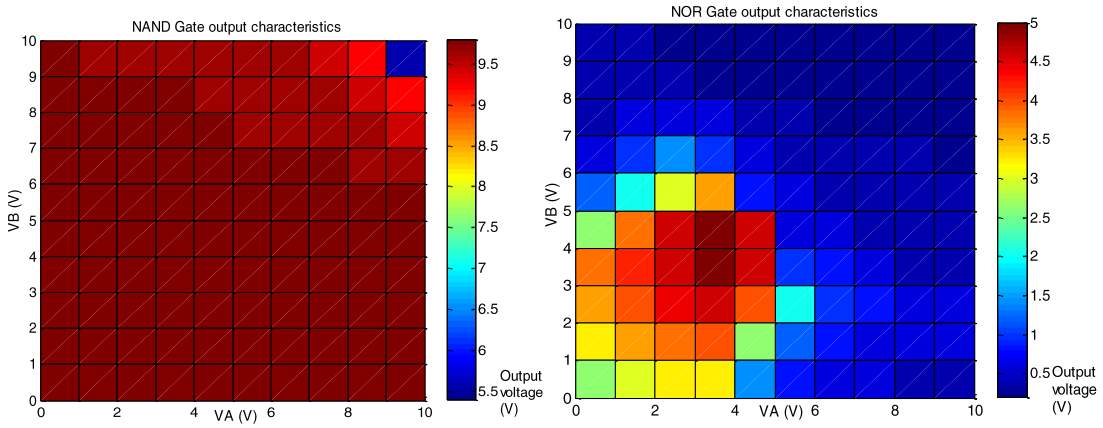
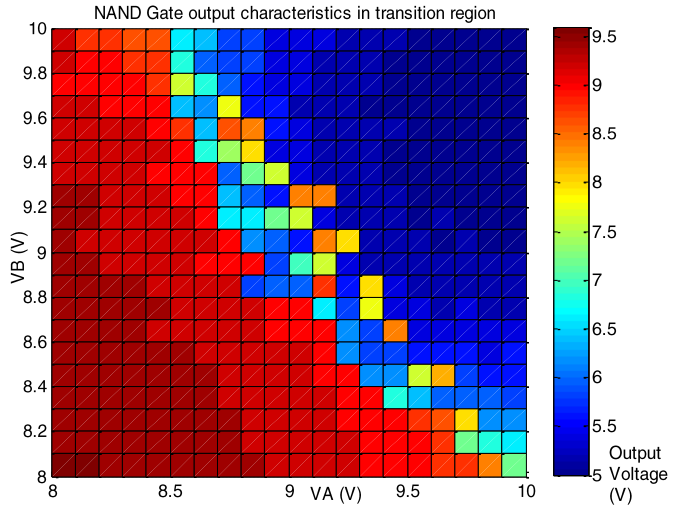
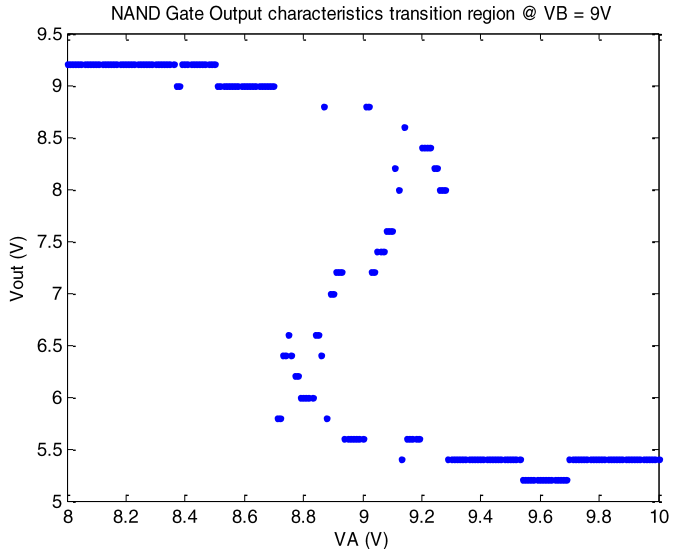


Figure S9 Simulated output charactersitics of graphene NAND and NOR gates: (a) NAND gate and (b) NOR gate, V_{DD}=10V.

To further investigate their performance, we zoom in the transition region and increase the step size. It turns out that there are even more stable states for a single input. For instance, as we can see in Fig S10, there are even more multi-stable states for a NAND gate compared with those for a NOT gate. This indicates that with the increase of circuit complexity, more and more multi-stable states will emerge which will add instability to the whole system.



(a)



(b)

Figure S10 Simulated output characteristics of a graphene NAND gate in the transition region. (a) The output voltage for different A and B inputs. (b) The output voltage versus input A with a 9V input B.

This might indicate that with the increase of circuit complexity, more and more multi-stable states will emerge which adds instability to the whole system.

Generally, in this situation, even if a proper bandgap is opened, graphene gates sit still outside from being suitable for real applications.

2. Calculation of RF Parameters

Nevertheless, graphene is also a promising material in radio-frequency applications; particularly, the NDR effect may extend the applications from high speed switches to more sophisticated integrated circuits. Recently, GFETs with cut-off frequencies as high as several hundreds of gigahertz have been reported [5, 28].

In general, the cut-off frequency which represents highest frequency unit gain can be obtained is derived as [18]

$$f_T = \frac{g_m}{2\pi\{(C_{gs}+C_{gd})(1+g_{ds}R_{SD})+C_{gd}g_mR_{SD}\}}$$

from the small signal equivalent shown in Fig. S11 a. Where the transconductance g_m, drain conductance g_{ds}, gate-drain capacitance C_{gd} and gate-source capacitance C_{gs} are respectively defined as follows:

$$g_m = \frac{dI_{ds}}{dV_{GS-top}}|_{V_{ds}=const.}; g_{ds} = \frac{dI_{ds}}{dV_{ds}}|_{V_{GS-top}=const.}$$

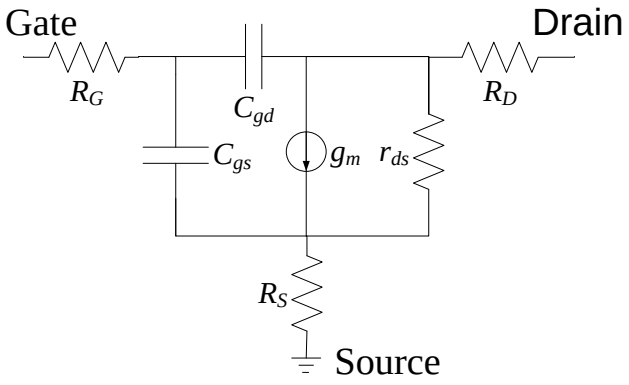
$$C_{gs} = -\frac{dQ_{ch}}{dV_{GS-top}}|_{V_{ds}=const.}; C_{gd} = -\frac{dQ_{ch}}{dV_{ds}}|_{V_{GS-top}=const.}$$

Here, the overall channel charge Q_{ch} is calculated by integrate the sheet concentration along the whole channel

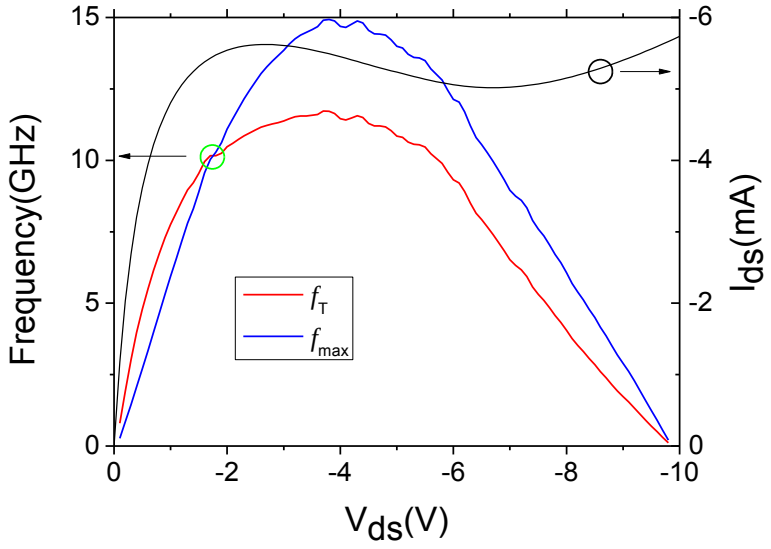
$$Q_{ch} = qW\int_0^L \mathrm{sgn}(V_{ch}(x))\rho_{sh}(x)dx$$

The integration is carried out by transferring the spatial dependence of the sheet concentration to the chemical potential space, by utilizing:

$$\frac{dx}{dV_{ch}} = \frac{dx}{dV}\frac{dV}{dV_{ch}} = (\frac{q\rho_{sh}\mu W}{I_{ds}} - \frac{\mu}{v_{sat}})(-1-\frac{k|V_{ch}|}{C_T+C_B}).$$



(a)



(b)

Fig. S11 (a) Small signal equivalent circuit of a GFET. (b) Simulated f_T and f_{max} versus applied drain-source voltage, for GFET in Ref [9] under a -1.25V top gate and -40 V back gate bias. Also shown is the simulated drain-source current.

By utilizing this model, the simulated *extrinsic* cut-off frequency of the GFET in Ref [9] under -1.25V gate voltage is shown in Fig. S11 b. Benefited from the high mobility, a more than 10 Ghz peak of f_T occurs around the saturation region for this 1 μm transistor.

In addition to the cut off frequency, another important figure of merit in RF applications is the maximum oscillation frequency, which is defined as the highest frequency where power gain is one and can be expressed as

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}(R_G + R_{SD}) + 2\pi f_T R_G C_{gd}}}$$

Owing to fact that the current saturation is very weak in linear or kink regions, only relatively low operation frequencies have been achieved in graphene RF integrated circuits although the cut-off frequency is relatively high [29]. Without a bandgap, the saturation condition (pinch-off channel with a bandgap in most MOS FETs) is also very hard to be created in graphene. As a result, the RF performance of GFET is limited so far. Fortunately, by exploiting NDR effect, the f_{max} can be dramatically enhanced, which is easily understood by considering the denominator of the above equation. Negative g_{ds} yields smaller denominator and thus higher f_{max}. Fig. 11 b shows the simulated f_{max}. In NDR region, the extrinsic f_{max} reaches 30 GHz and is much higher than f_t, in stark contrast to the lower f_{max} in traditional linear region which is observed in most cases.

Interestingly, in the negative gds cases, the parasite resistance further decreases the denominator. Therefore, the unfavorable high contact resistance actually helps to increase the f_{max}. Accordingly, NDR effect provides a possible solution for graphene based RF applications, in spite of which need to be future experimentally verified.