

## Electronic Supporting Information

### Highly crystalline single Au wire network as high temperature transparent heater

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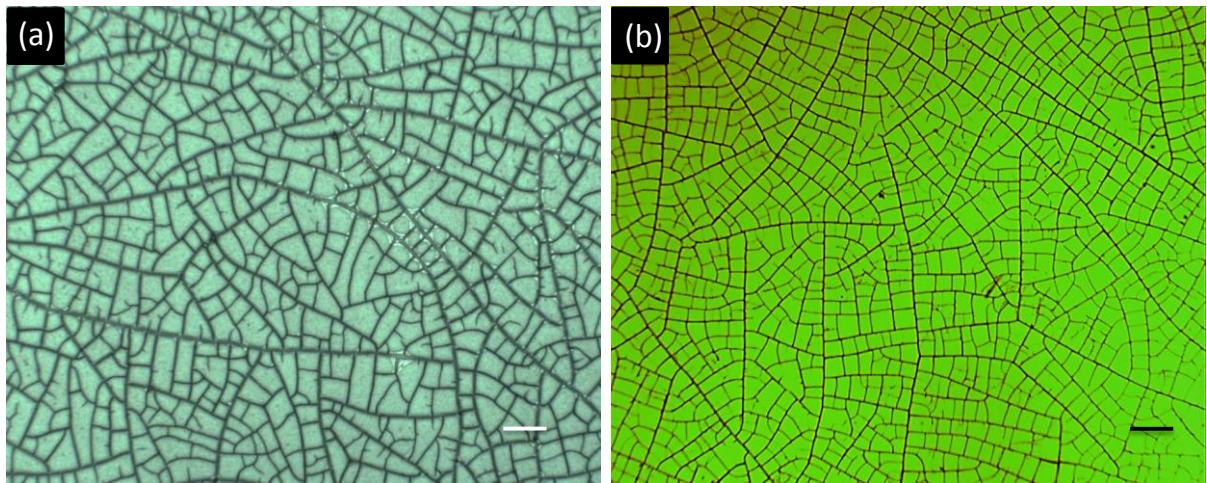


Fig. S1: Optical micrographs of a) Crackles formed in acrylic resin film and (b) Single Au micro/nano wire network, after deposition of Au metal and liftoff (Scale bar 50  $\mu\text{m}$ ).

A 60  $\mu\text{l}$  of acrylic resin solution (0.4 g/ml) was drop coated on quartz and allowed to dry in air. The crackles formed spontaneously in a dried layer of acrylic resin as shown in Fig. S1. The crackles are typically few micron to sub-micron wide and are highly interconnected across the large area, crucial for metal wire network formation in the final step.

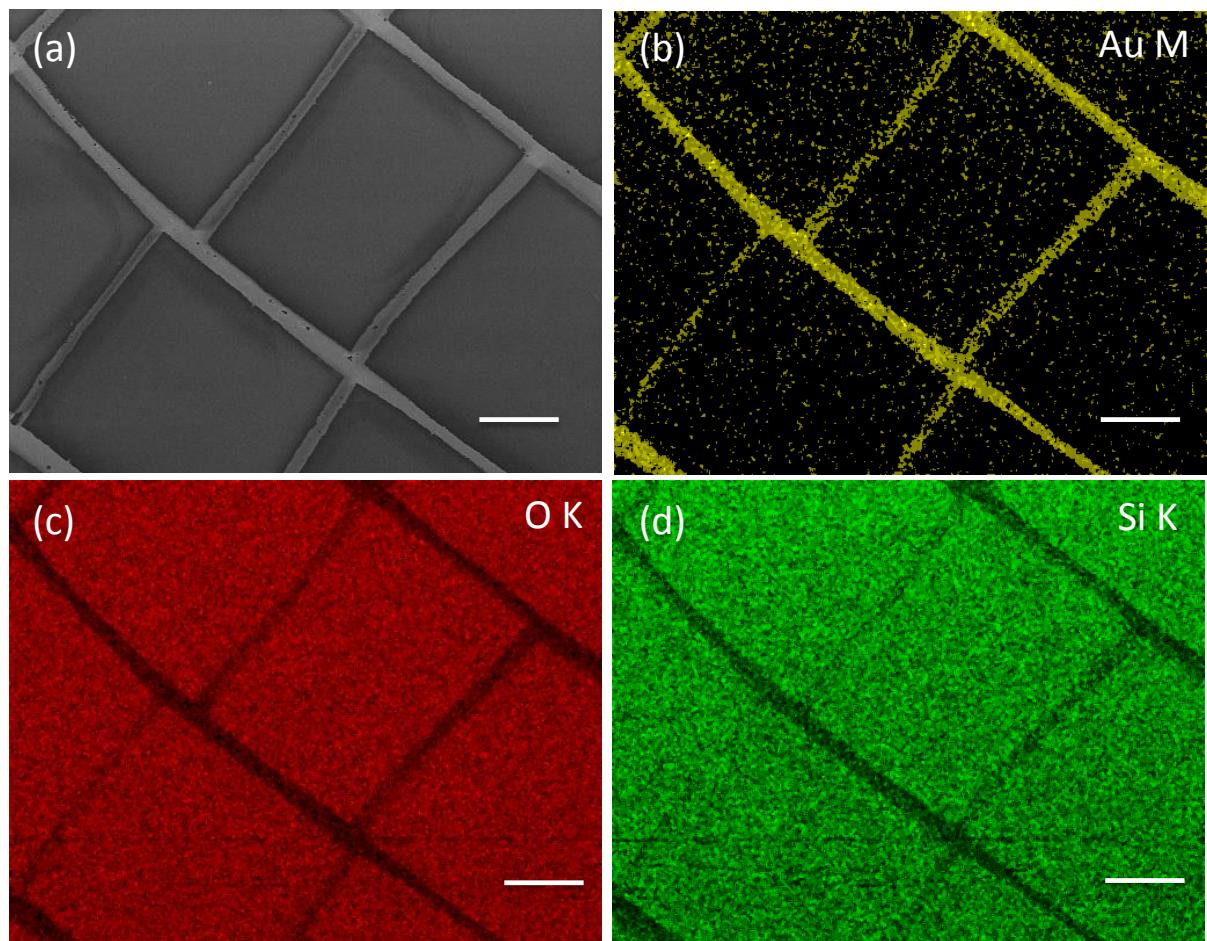


Fig. S2: (a) SEM of image of Au network on quartz substrate, EDS maps of the same region corresponding to (b) Au M, (c) O K and (d) Si K, respectively (scale bar 10  $\mu$ m).

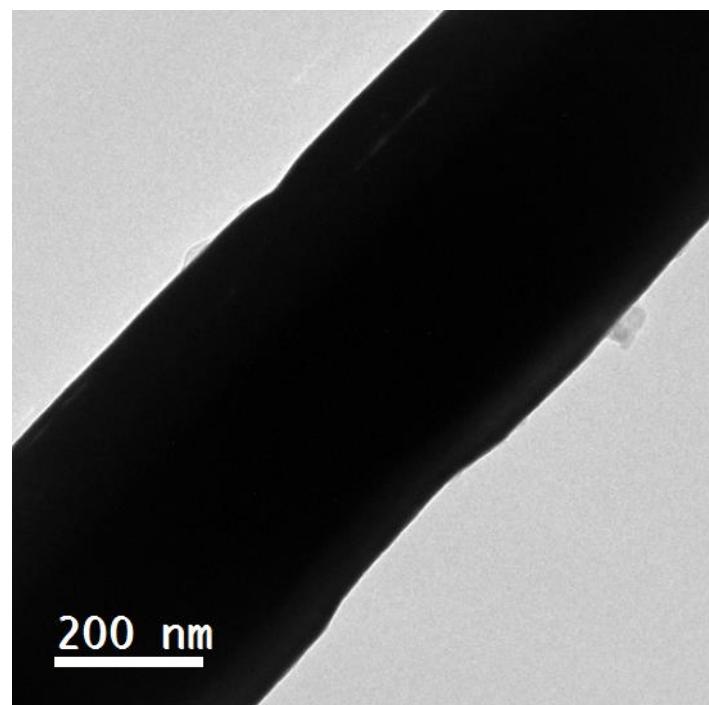


Fig. S3: Bright field TEM image of Au nanowire with width  $\sim$  500 nm.

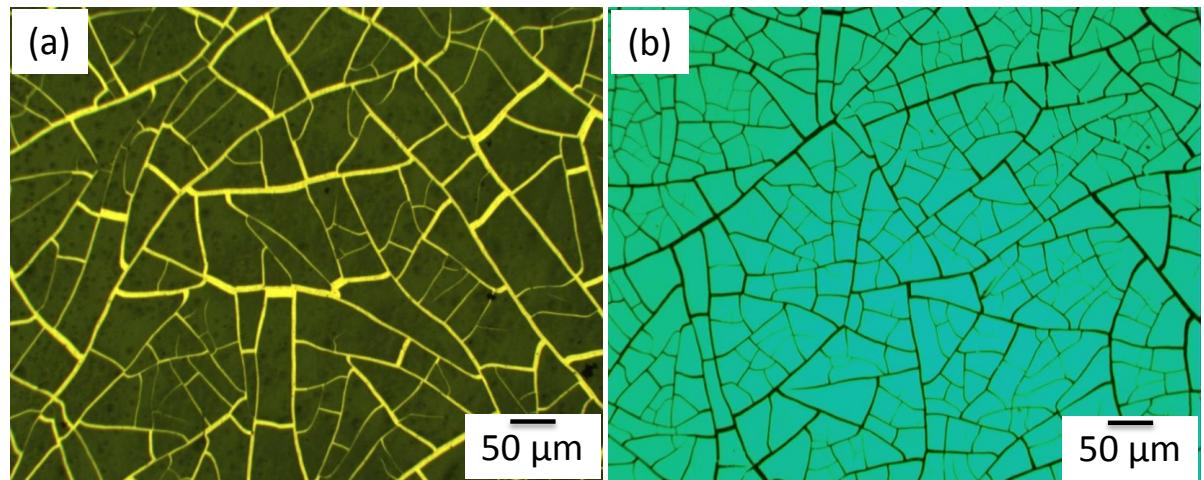


Fig. S4: Optical micrographs of (a) Au network on PET substrate (reflectance mode) and (b) Ag network on glass substrate (transmittance mode).

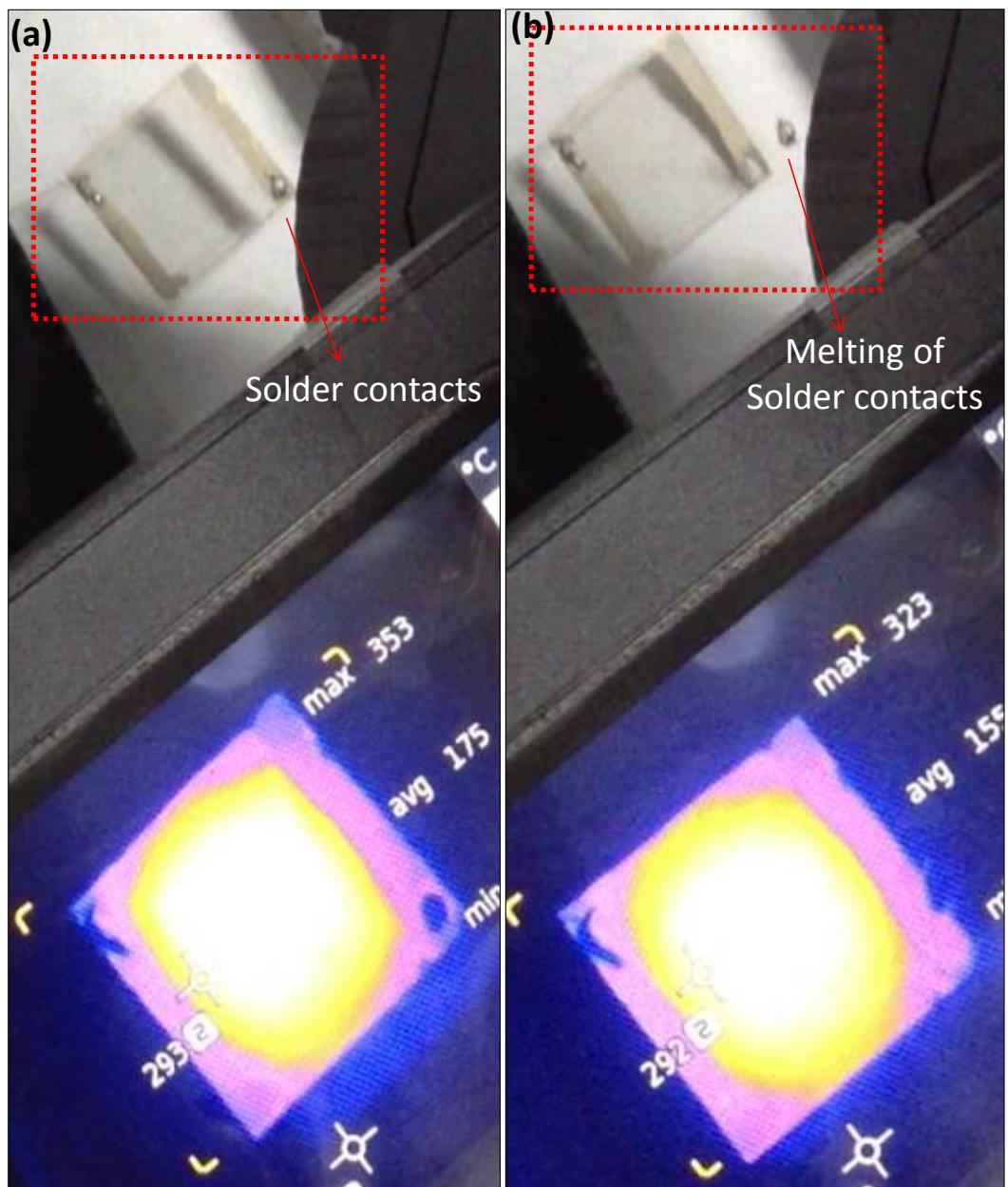


Fig. S5: Transparent heater with solder as contacts (a) before and (b) after melting of the solder. As the temperature increased the melting temperature of the solder ( $250\text{ }^{\circ}\text{C}$ ), the contact came off. Temperature can be read from the IR camera screen.

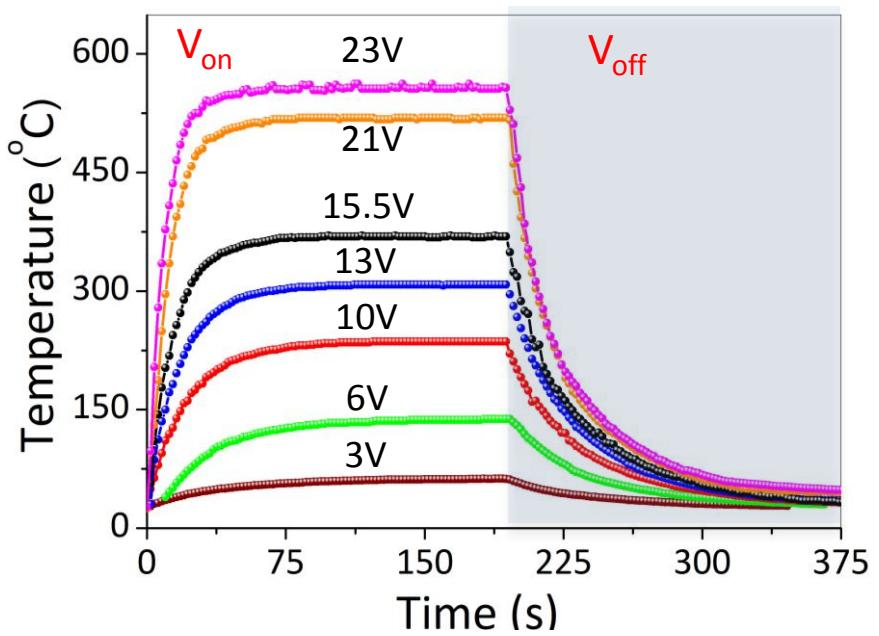


Fig. S6: Temperature profiles of Au wire network/quartz as a function of time at different applied voltages recorded using an IR camera (Au wire thickness 60 nm).

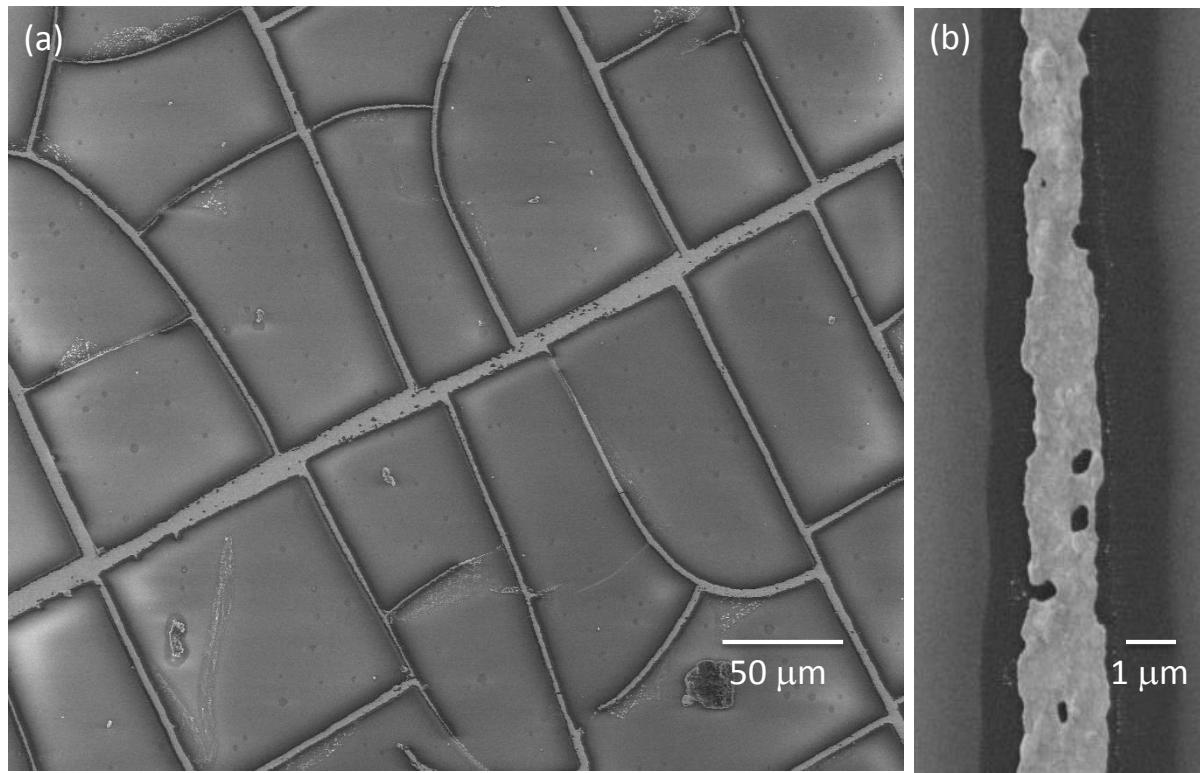


Fig. S7: (a) SEM image of damaged Au wire network after self-annealing 650 °C, (b) A magnified view showing pinholes.

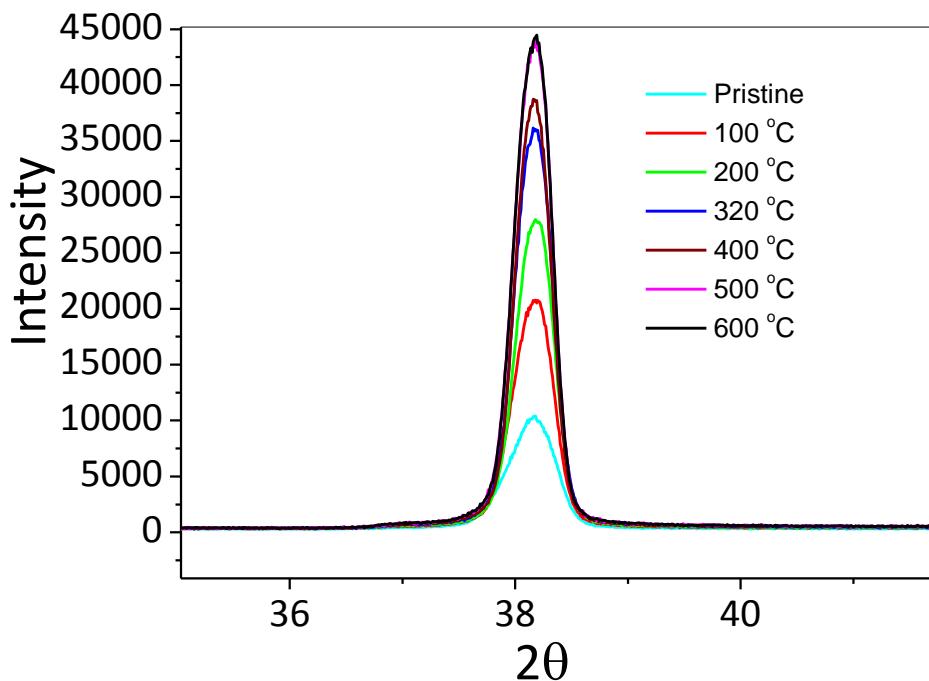


Fig. S8: XRD of Au wire network after annealing at different temperatures.

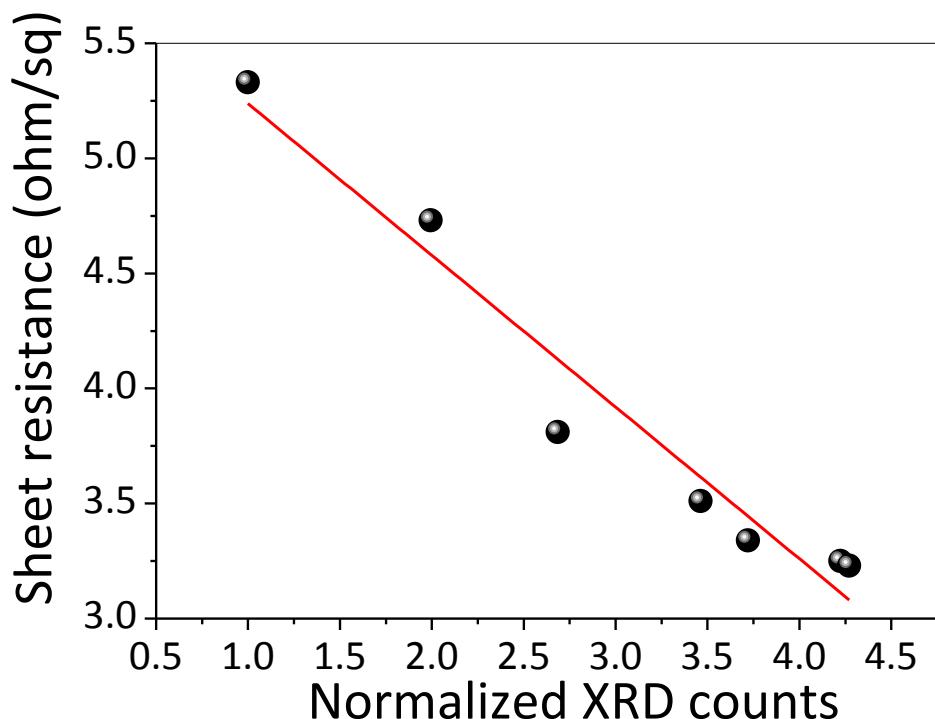


Fig. S9: Sheet resistance as a function of normalized XRD counts, solid circles are experimental data and red line is a linear fit. The reduction in the sheet resistance value is attributed to increase in the crystallinity of Au wire.

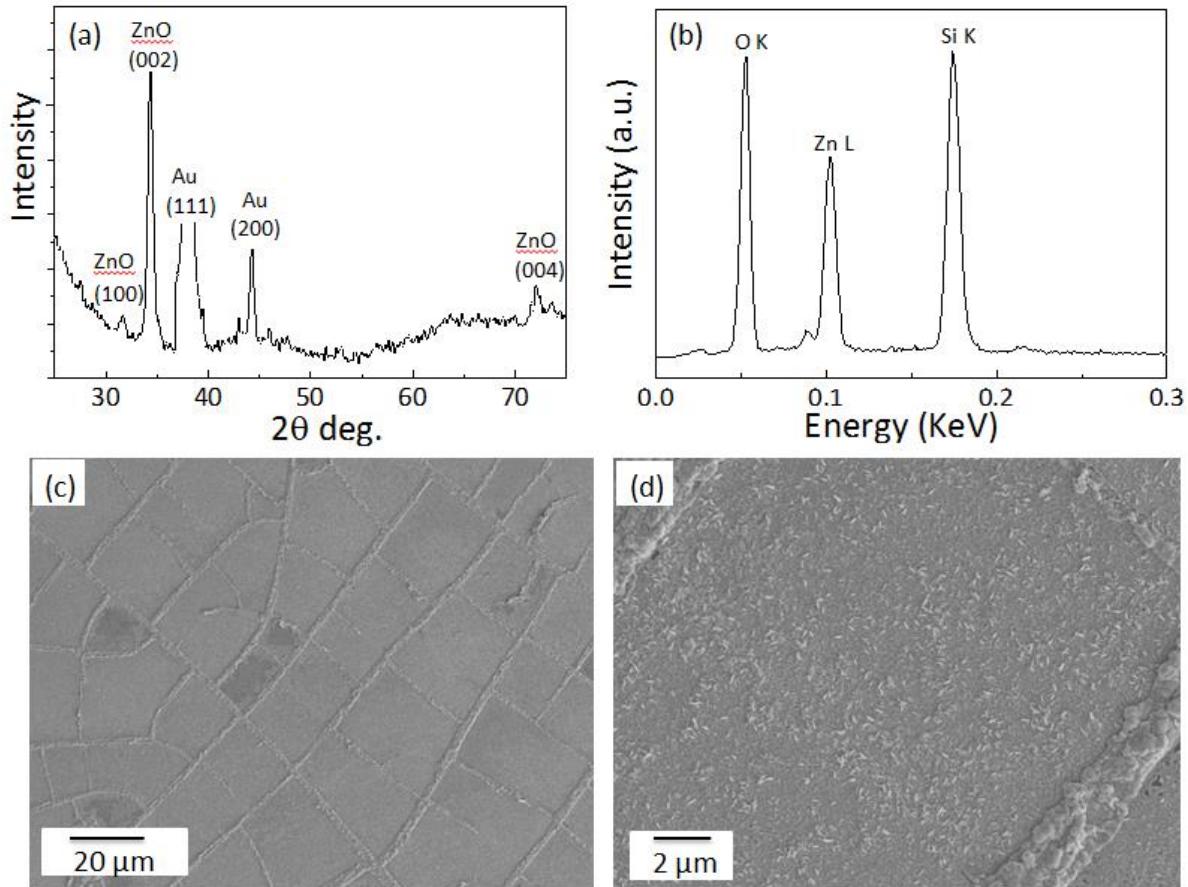


Fig. S10: ZnO thin film on Au network (HT-TCE): (a) XRD pattern and (b) EDS spectrum of ZnO obtained by oxidising Zn film in air by joule heating the Au wire HT-TCE to 450 °C for 45 min. (c) SEM image of ZnO thin film fabricated on Au network, (d) a magnified view.

In this experiment, the Au wire HT-TCE has been used as joule heater to prepare ZnO film starting with Zn film, just as an example. A Zn thin film (thickness,  $\sim$  60nm) was deposited on the Au wire HT- TCE. By applying a bias of 9V, the HT-TCE was heated to 450 °C in air when Zn oxidation began. After 45 min, the substrate was cooled. The XRD pattern (see Fig. S10(a)) clearly demonstrates the formation of ZnO. The EDAX spectrum in Fig. S10(b)) reveals the formation of ZnO on Au wire HT-TCE. The SEM images show (see Fig. S10(c) and (d)) that the Au wires are buried beneath the ZnO thin film. The overall roughness of the Au wire TCE was found to be 60 nm for wire thickness of  $\sim$  220 nm, which decreased to  $\sim$

30 nm after ZnO film formation. Such barrier layers are required for the fabricate of optoelectronic devices.

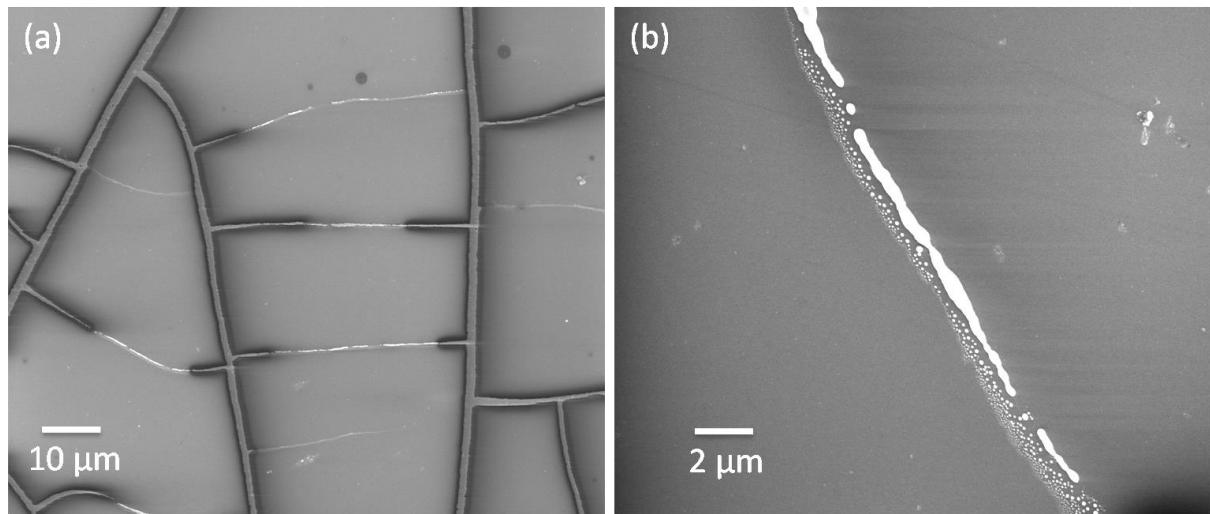


Fig. S11: (a) SEM images of externally heated Au wire network (450 °C for 30 minutes), (b) magnified view, demonstrating dewetting.

Table-S1: Summary on FOM values of Au wire network based TCEs

S.No	Thickness of Au network (nm)	T(%)	$R_s$ ( $\Omega/\square$ )	Figure of merit
1	60	86.6	5.4	472
2	220	87.2	3.1	858

Table S2: TCEs as transparent heaters. ITO, thin film as well as nanowire/nanotube network based TCEs from the literature compared with Au wire network/quartz from this study

S.No	Material used	Applied Voltage (V)	Maximum temperature achieved (°C)	Response time (s)	$R_s$ ( $\Omega \square^{-1}$ )	Remarks	Ref
1	Ag NW	7	55	500	33	Thermal annealing is required to decrease the contact resistance	<sup>1</sup>
2.	Ag NW	7	100	75	10	-----	<sup>2</sup>
3.	Graphene	12	100	75	43	Graphene is required to dope with Au	<sup>3</sup>
4.	Graphene	12	100	300	66	Graphene is required to dope with Au	<sup>4</sup>
5.	MWNT	15	75	---	349	High sheet resistance	<sup>5</sup>
6.	SWNT	60	160	---	139	Thermal heating is required	<sup>6</sup>
7.	SWNT	60	47	60	2600	High sheet resistance	<sup>7</sup>
8.	SWNT	60	200	~70	250	Transmittance is only 30 %	<sup>8</sup>
9.	ITO	50	180	25		Films are not flexible	<sup>9</sup>
10	ITO	20	160	110	633	Sintering at 400 °C is required	<sup>10</sup>
11.	Ga doped ZnO	42	90	30	---	thin films	<sup>11</sup>
12.	Ga doped ZnO	20	160	50	---	thin films	<sup>12</sup>
13.	Ag NW / SWNTs	15	100	30	---	Hybrid structures	<sup>13</sup>
14.	MWNT	40	140	30	172	5 layers of MWNTs were used	<sup>14</sup>
15	Graphene	60	180	120	641	Annealing at higher temperatures	<sup>15</sup>
16.	Au wire network/quartz	23	550	45	5.4 & 3.2	Au thickness = 60 nm	Present work
		12	600	40	2.44 & 3.3	Au thickness = 220 nm	

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**Movie S1:** Soldering lead melting using transparent heater