Supporting Information

Selective Functionalization and Loading of Biomolecules in Crystalline Silicon Nanotube Field-Effect-Transistors

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1. Methods for Ge/Si core/shell nanowire growth and nanotube synthesis

Ge/Si core/shell NWs were grown on Si (100) wafers by the well-known vapor-liquid-solid (VLS) process using low-pressure chemical-vapor-deposition (ET-2000, CVD Corporation)[26,27]. Colloidal Au nanoparticles of 5-80 nm were dispersed on Si substrates as catalyst for Ge core growth using 1.8% GeH_4 in H_2 (300 Torr total pressure, 290°C). Subsequently, in-situ deposition of epitaxial, crystalline Si shells was carried out using 2% SiH_4 (30 Torr, 600°C) with varying growth duration depending on the desired shell thickness. During Si shell growth diborane (B_2H_6) was used as in-situ doping source at a flow rate of 20 sccm and a B:Si atomic ratio of 1:560. As a comparison, amorphous Si shells were grown using a lower temperature at 490 °C. Following growth of core/shell NWs, Si NTs were made by selective wet etching of Ge cores using 30% hydrogen peroxide with an etch rate of ~760 nm/min at 60°C. A series of centrifugal filtration (Nanosep 30K MWCO, Pall Co.) in isopropyl alcohol (IPA) were used to purifie the resulting NTs.

2. Determining gate capacitance of Si NT FETs

To find C_G we used finite element electrostatic simulation coupled with the equation:

$$\varepsilon_r \varepsilon_0 \nabla^2 V(x,y) = q\left[p(V) - n(V) + N_a\right]$$

to evaluate the potential V and hole carrier distribution in the cross-section of the NT or NW at different back-gate voltages in order to extract the gate capacitance. Here p, n and N_A represent hole density, electron density and unintentional doping/impurity doping density in the Si shell, respectively.

A cross-sectional view of the equipotential and hole carrier distribution is presented in Fig. S1b and c, for the cases of a nanowire and a nanotube, respectively. Both cases have the same outer diameter (40 nm), with the difference being the NT is hollow inside its 30 nm ID. If we assume a doping level N_A at 1×10^{17} cm^{-3}, Fig. S1b,c show that the hole carriers are mostly concentrated at the bottom surface and the outer circumference for both cases, regardless whether there is a void inside the NT. Indeed, as we experimented through a wide range of N_A levels, the resulting gate capacitance C_G is identical between NT and NW (Fig. S1a inset) and does not depend on N_A at on state (V_G = -20 V). This is a result of the screening effect from large amount of hole carriers distributed on the outer surface of the NW or NT, making both materials behave similar to a metallic cylindrical conductor. As Fig. S1a shows, C_G also remains relatively constant with V_G throughout most of the on-state and only decreases significantly at V_G > -3 V when the hole carriers are beginning to be depleted. Although in our experiments, the exact activated dopant level N_A is yet to be determined due to the c-Si FETs exhibiting enhancement mode (normally-off) FET behavior, since C_G is insensitive to N_A as our simulation shows, we can use C_G = 3.37 fF to extract the on-state field effect mobility of the device in Fig. 2.

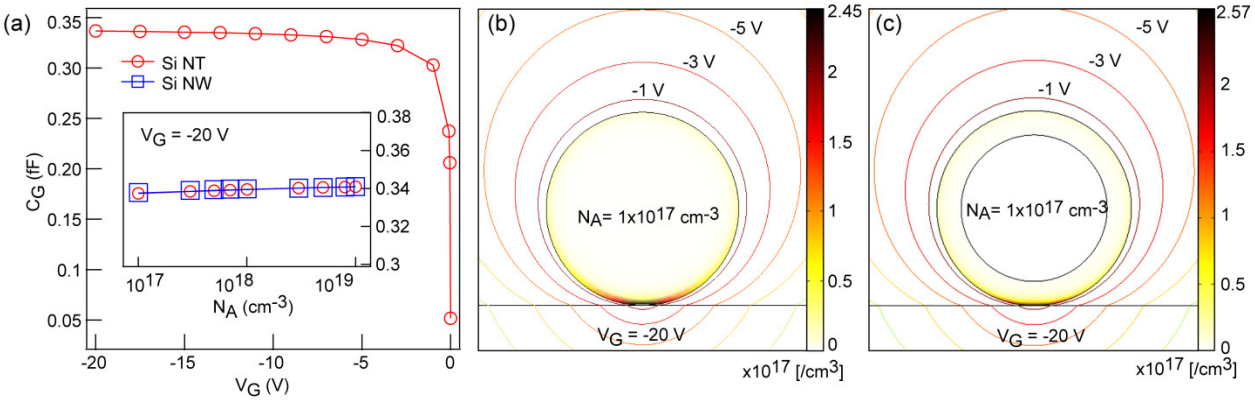

Figure S1. Two-dimensional finite element electrostatic analysis of gate capacitance for NT and NW structure using COMSOL Multiphysics. (a) Calculated gate capacitance of a NT on 100 nm thick gate oxide with 30 nm ID, 5 nm shell thickness and 7.3 μm in length as a function of applied gate bias. The inset represents gate capacitance versus

doping level at V_G= -20 V. (b, c) Comparison of calculated gate capacitance between Si NT and NW from FEM modeling. Space charge distribution (colored scale) and equipotential profile (lines) of (b) Si NW and (c) Si NT at carrier concentration of 1×10^{17} cm^{-3} and gate bias of -20 V.

3. Methods for PEGylation of Si NT surface

The surface of as-grown Ge/Si core/shell NWs was first cleaned and activated by a UV cleaner (Jelight, model 42) for 20 min. The growth wafer then reacted in trimethoxysilane PEG solution (2 mg in 200 µl toluene) for 30 minutes, followed by rinsing with toluene and acetonitrile for three times. It is worth noting that both the growth substrate and the NWs outer surface were covered in this step during PEGylation. The entire growth substrate was then sonicated in isopropyl alcohol (IPA) to break off the PEG-encapsulated NWs from the substrates and to expose clean, naked terminals of the Ge core to allow for the subsequent Ge core etching. The etching step was performed in the solution of IPA/30% hydrogen peroxide 3:1 v/v at 60 °C for 3 hours.

4. Methods for functionalization of the SiNT inner surface with Rhodamine dye

First, Si NTs with PEG on the outer surface were centrifuged to exchange buffer solution with DI water using a 30K MWCO centrifuge filter. Subsequently, inner surfaces of Si NTs were hydraoxylated with 2M nitric acid, then coated with 3-aminopropyltriethoxysilane (APTES) as a self-assembled monolayer to enable the covalent bonding to the carboxylic group on Rhodamine. 2 % (v/v) APTES was added to the Si NTs solution and reacted for 4 hours. Excessive APTES was removed by a 100K MWCO centrifuge filter. The purified solution was mixed with 5 mM Rhodamine dye (Sigma-Aldrich) in methanol and kept reacting overnight. After reaction, excess Rhodamine dye was removed by using 30K MWCO centrifuge filter and the functionalized Si NTs were dispersed in DI water.

5. Methods for functionalization of the SiNT inner surface with FITC-modified BSA

To synthesize BSA-FITC conjugates, thiol-maleimide coupling chemistry was used. BSA was dissolved at 20 mg/mL in pH 7.0 10 mM phosphate buffer. Disulfide bonds in BSA were reduced by 100 fold excess of dithiothreitol (DTT) for 20 min. Excessive DTT was removed by desalt column (Thermo Scientific). DTT treated thiol-BSA was then reacted with maleimide-FITC for overnight, and the resulting BSA-FITC was purified by 30K MWCO centrifuge filtration.