Electronic Supplementary Information (ESI) available:

Exploration of yttria film as gate dielectric in sub-50nm carbon nanotube field-effect transistors

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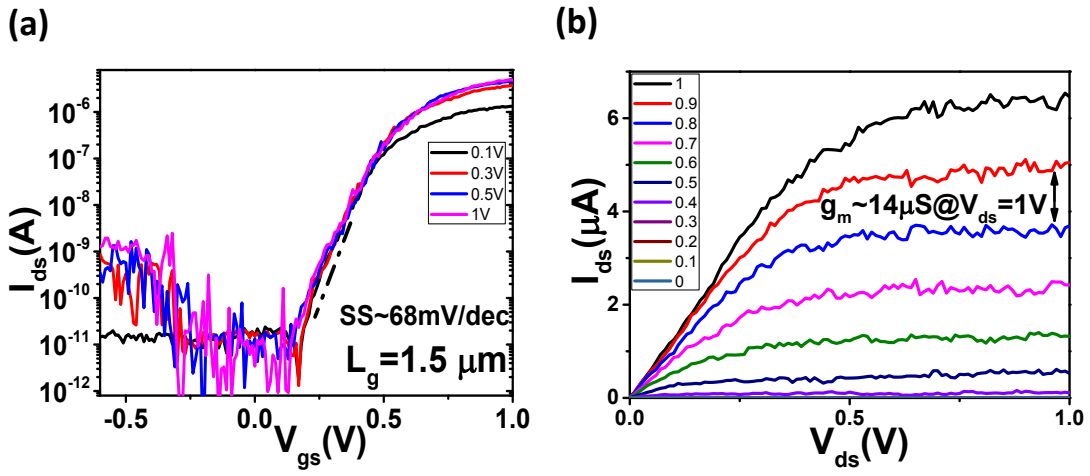

Figure S1. Electrical properties of typical CNT FETs using Y_2O_3 film as gate insulator with gate length about 1.5 μm. (a) Transfer characteristics of this typical long gate FET and its (b) Output characteristics. The Vgs varies from 0 to 1.0 V from bottom to top with a step of 0.1 V.

Device leakage current and hysteresis

Low leakage current is also an important property for high-quality gate insulator, and then all of the gate voltage dependent gate leakage current (I_g-V_{gs}) curves of the CNTFETs are measured and plotted. Shown in Fig. S2(a) are the I_g-V_{gs} curves of all long gate CNTFETs, whose leakage currents are at order of tens pA which demonstrates nearly no leakage current. Only one device possesses leakage current about hundred pA at V_{gs} close to 1 V probably owing to existence of random defects in the Y_2O_3 film formed during the fabrication process. Compared with long channel devices, short channel devices present much smaller leakage current (all below 8 pA) as shown in Fig. S2(b) since decreased gate length (smaller dielectric layer size) will lower the possibility of leakage. Leakage current and break down field is mainly determined by the property, the quality and thickness of dielectric. As ideal material of yttria, its insulating property is perfect due to the characterization of our high quality yttria (as shown in Figure 3c and 3d), and the break down field is at least the same (larger than 4 MV/cm) as that in ref 28.

Small hysteresis in transfer curve indicates few charge traps located near the CNT/Y_2O_3 layer interface or within gate insulator and then is another character of high-quality gate insulator in FETs. In order to further characterize Y_2O_3 dielectric layer qualitatively, transfer curves of one long and one short gate CNTFETS are measured through sweeping V_{gs} forward and then back as shown in Fig. S3. It is obvious that hysteresis both in long gate and short gate CNTFETs is very small (<80 mV). It is should be noted that the hysteresis is nearly not dependent on bias voltage as Figure S3a shows for long channel devices and a minor degradation from 60 mV @ 0.1 V bias voltage to 80 mV @ 0.5 V bias voltage exists shown in Figure S3b for short channel devices, which indicates that the interface between CNT and gate insulator is very clean.

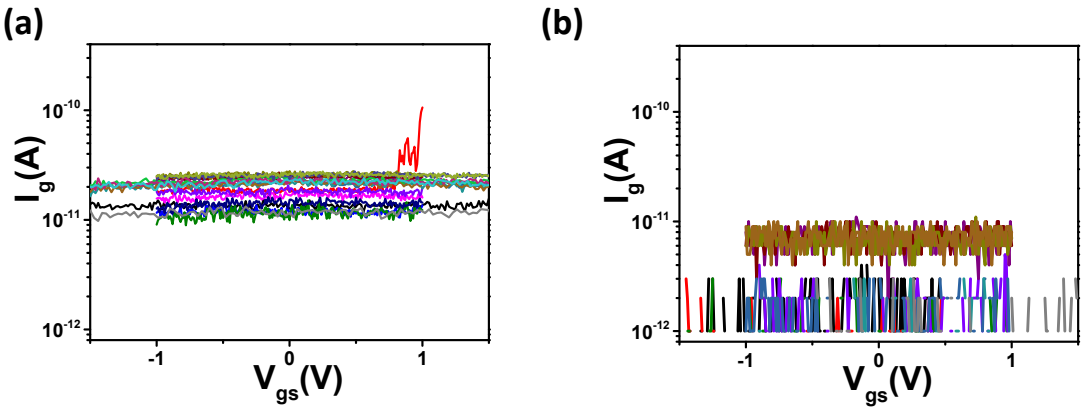

Figure S2. Leakage current characterization for long and short gate length devices. (a) for long gate length devices (1.5 μm), leakage currents are at order of tens pA which demonstrates nearly no leakage current. (b) for short gate length devices (~ 50 nm), leakage currents are much smaller than that long ones and are all below 8 pA.

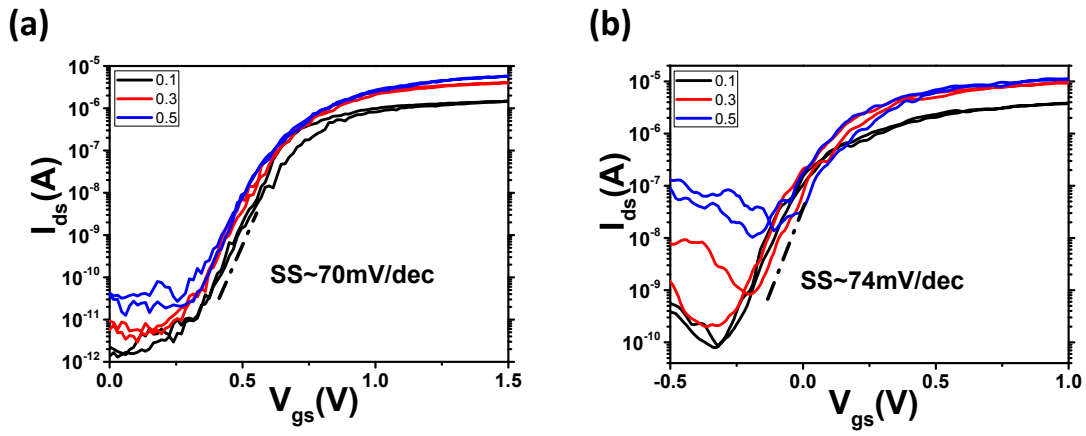

Figure S3. Hysteresis characterization for long and short gate length devices. (a) for long gate length devices (1.5 μm), almost no observable hysteresis exists. (b) for short gate length devices (~ 50 nm), the hysteresis is less than 80 mV.

On- and off-state Current Ratio

From the On- and off-state current shown in Fig. 2(c) and 2(d), we also calculate the On- and off-state current ratio for both short gate and long gate devices shown in Fig. S4(a) and S4(b) respectively. 10 short gate devices are all from devices shown in Fig. 1(e) while 16 long gate devices are from devices shown in Fig. 1(f). Compared to 19 devices in Fig. 1(f), 3 devices data is missing because transfer curves under 0.5 V bias voltage of that 3 devices are not measured. Consistently with On- and off-state current in Fig. 2(c) and 2(d), on/off ratio of short gate and long gate devices are mainly located from 10 to 1000 except one long gate device up to 4000. For short gate devices, there are 60% devices (6/10) ratio between 10 and 100 while 40% (4/10) devices ratio between 100 to 1000. For long gate devices, there are 50% (8/16) devices ratio between 10 and 100 while 43.7% (7/16) devices ratio between 100 and 1000. It is worthy of noting that short gate devices and long gate devices are almost with same ratio statistics result indicating that our devices with yttria are of great gate control ability even scaling gate length to about 50 nm.

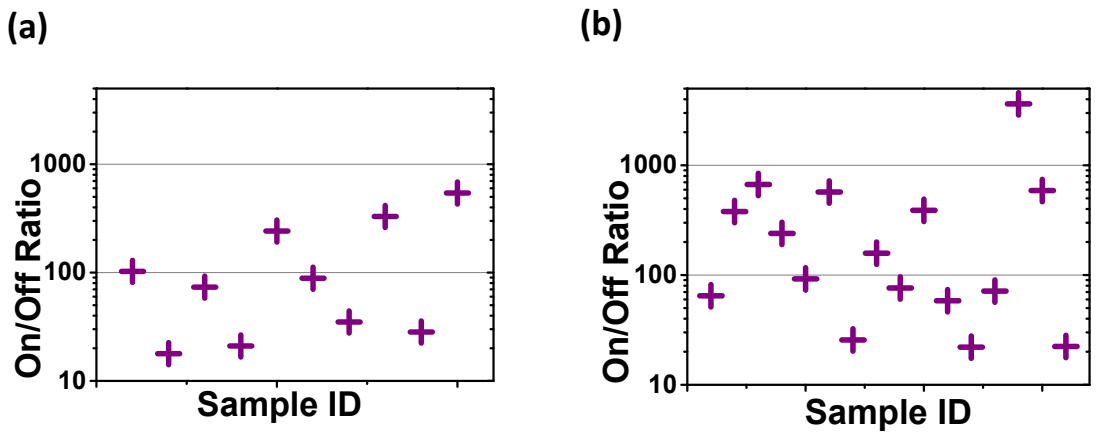

Figure S4. Statistics result of On- and off-state current ratio for 10 short gate devices (a) corresponding to Fig. 1(e) and 16 long gate devices corresponding to Fig. 1(f). The On- and off-current extraction method is the same as in Fig. 2.

XPS characterization

XPS measurement is carried out at three different depth of 0, 2 and 6 nm from sample surface. Typical surface scan result is shown in Fig. S5(a). The absolute content of elements is area under element curve. According to Fig. S5(a), four elements are detected from XPS measurement, and their atomic percentage is shown in Fig. S5(b). In order to obtain relative atomic percentage of Y:O, we need remove part of element O which is brought from other oxides such as silicon oxide and so on. Detailed scan curves of element Y and O with three different depths are shown in Fig. S5(c) and S5(d). As we can see, the content of Y increases and that of O decreases from exposed surface because it is harder for O to penetrate as depth increases. But at 6 nm depth, which is around the interface between yttria and silicon oxide, the content of O increases sharply owing to the the contribution of O from silicon oxide substrate. From Fig. 2 of text, the whole yttria layer is oxidized completely to form continuous polycrystalline structure after our efficient oxidation process indicating excellent film quality of yttria.

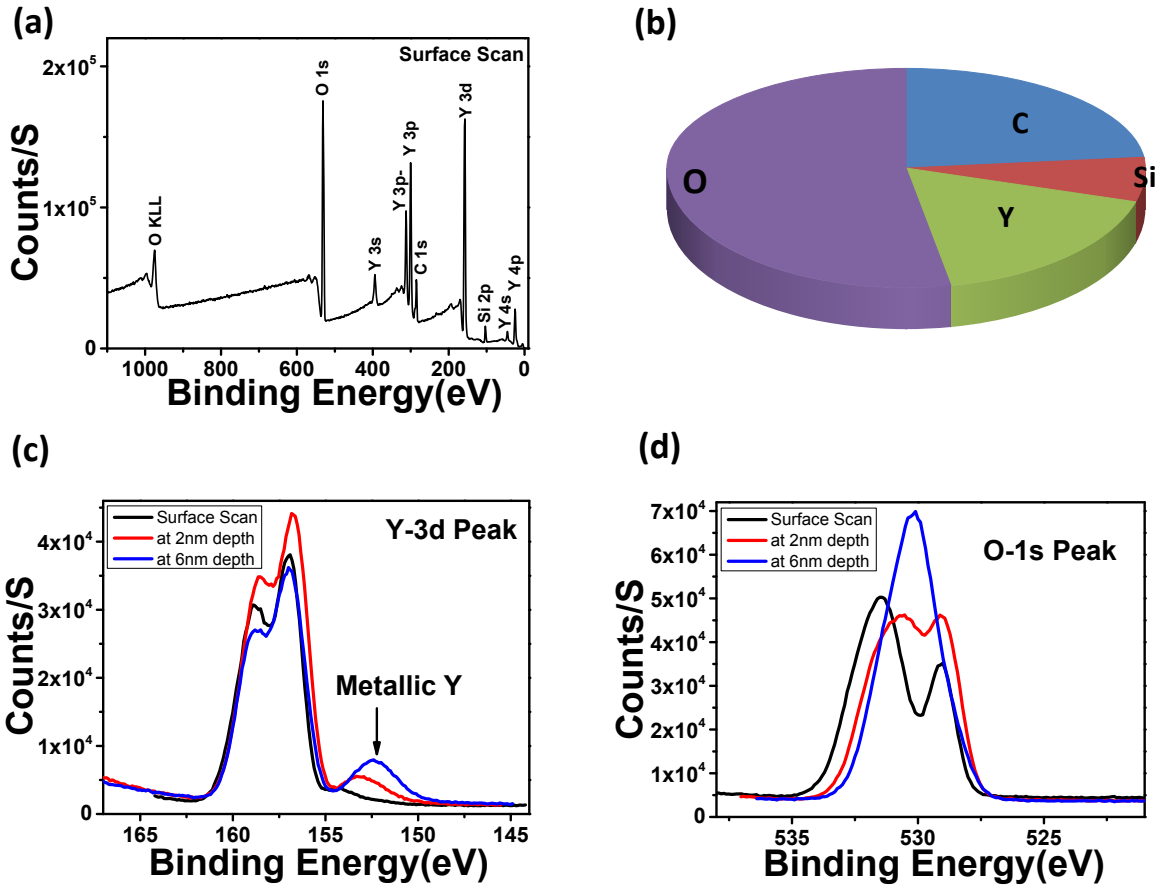

Figure S5. XPS characterization of this yttria film at three depth, 0 nm, 2 nm and 6 nm from yttria surface. (a) is surface scan of yttria showing all detected elements and corresponding atomic percentage is shown in (b). 2 nm scan and 6 nm scan are omitted for their similarity with only different atomic percentage. Detailed scan curves of element Y and O with three different depth are shown in (c) and (d). As depth increases, the content of Metal Y gradually increases while slightly decreasing content of O is observed except for at 6 nm depth owing to the contribution of O from silicon oxide substrate.