## **Supplementary Information**

## On-Chip High Power Porous Silicon Lithium Ion Batteries with Stable Capacity over 10,000 Cycles

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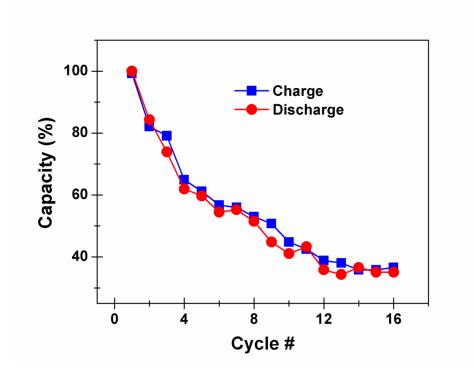
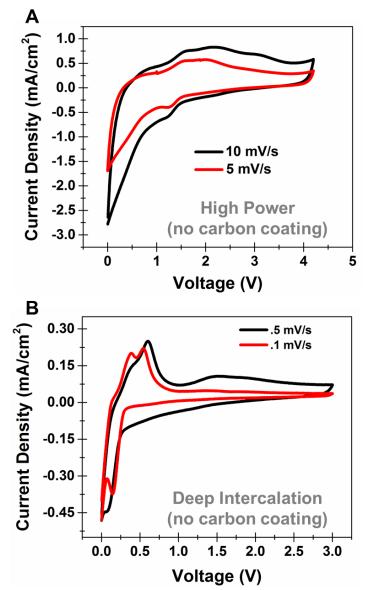
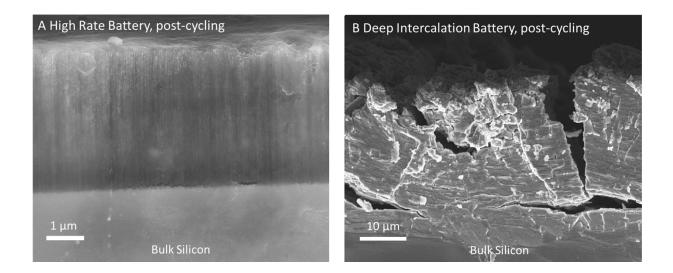


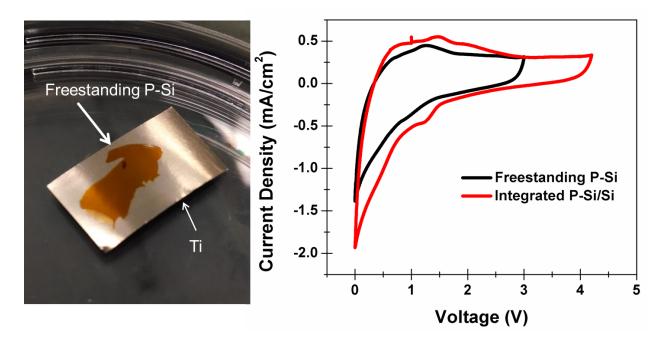
Fig. S1. Capacity as a function of cycle number for carbon passivated porous silicon anodes cycled at  $1 \text{ mA/cm}^2$ , where intercalation deep into the silicon bulk is observed. Notably, the capacity fades rapidly with ~ 60% capacity loss over the first 16 cycles.



**Fig. S2.** CV curves showing both (A) high power lithium storage and (B) standard deep intercalation storage in porous silicon materials not passivated with carbon. Notably, in (A), we observe a charge-discharge redox pair similar to that observed in carbon passivated porous silicon materials, indicating the charge storage observed in Fig. 2 is associated with storage in the silicon material.



**Fig. S3.** Cross sectional scanning electron microscope (SEM) images of two porous Si batteries after 3000 cycles at high rate (A) and after 20 cycles at slow charging rates (B). Evident from (A) is the in-tact nature of the porous silicon material. In this sample, no damage or degradation was observed in the silicon material underneath the porous layer, and the nanostructured silicon in the porous layer exhibits no significant structural modications. From (B), lithium evidently intercalates deep into the bulk of the silicon material, causing the bulk silicon to pulverize and the capacity to rapidly fade.



**Fig. S4.** Comparison of lithium storage characteristics of freestanding P-Si layers. (left panel) Photograph of the substrate utilized, where the orange-colored material is a freestanding porous silicon layer produced by an electropolishing step following electrochemical etching as described in the main text. In the electropolishing step, a current density of 200 mA/cm<sup>2</sup> was pulsed for 15 seconds, and the porous layer was partially removed. The sample was then placed in an ethanol solution and agitated until a freestanding layer was isolated, and this was then dried on a Ti foil substrate as a battery electrode, and carbonized using an identical CVD process as that described

in the main text. This electrode Li storage performance was then assessed using cyclic voltammetry (right panel) at a rate of 5 mA/cm<sup>2</sup>, and normalized to the area of the porous silicon. Notably, due to the shape of the freestanding layer, and some delaminated regions during CVD treatment, we anticipate between 10 - 50% error in the absolute values of the current density. In comparison to the integrated P-Si/Si sample, the general high power behavior is the same – with no apparent bulk-like storage characteristics, and a redox couple at higher voltages. This indicates that the general high rate performance observed for integrated samples is due to the porous layer, clearly emphasized by the isolated freestanding porous layer showing the same Li storage behavior.