

# Supporting Information

## for

### Thickness-Dependent Mobility in Two-Dimensional MoS<sub>2</sub> Transistors

D. Lembke, A. Allain, A. Kis\*

*Electrical Engineering Institute, Ecole Polytechnique Federale de Lausanne (EPFL),  
CH-1015 Lausanne, Switzerland*

*\*Correspondence should be addressed to: Andras Kis, andras.kis@epfl.ch*

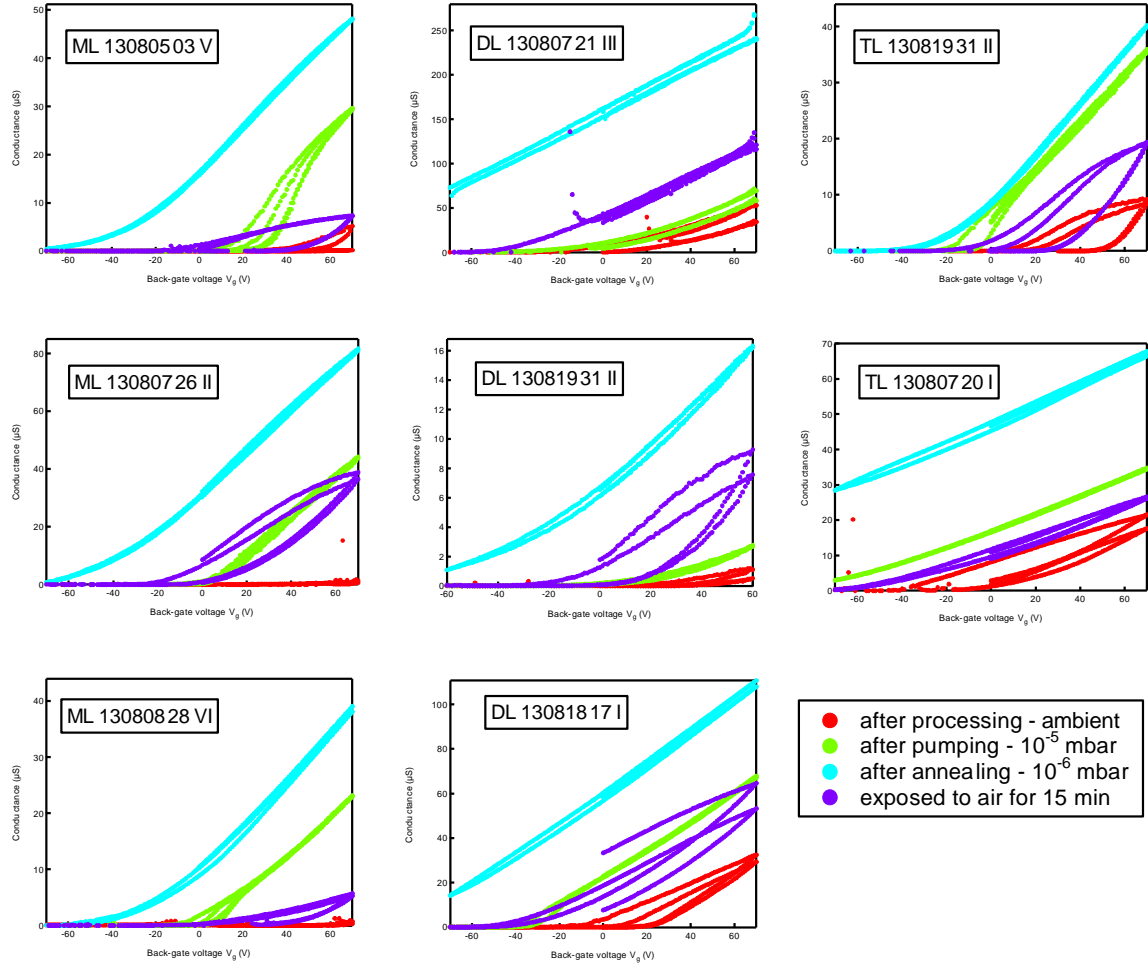
#### 1. Device Characteristics

In the table below, the following device characteristics are specified: device label, number (#) of layers, SiO<sub>2</sub> substrate unpolished or polished, length ( $L$ ), voltage probe spacing ( $L_{xx}$ ), width ( $W$ ), aspect ratio ( $L_{xx}/W$ ) as well as MoS<sub>2</sub> area ( $L_{xx} \cdot W$ ) exposed to ambient.

Label	#	Polished?	$L$ [μm]	$L_{xx}$ [μm]	$W$ [μm]	$L_{xx}/W$	$L_{xx} \cdot W$ [μm <sup>2</sup> ]
130805 03 V	1	no	7.0	4.0	2.4	1.66	16.8
130807 26 II	1	yes	3.2	1.4	1.3	1.08	4.2
130808 28 VI	1	yes	6.1	3.7	2.4	1.54	14.6
130807 21 III	2	yes	2.9	1.0	2.4	0.42	7.0
130818 17 I	2	no	5.4	3.4	2.4	1.42	13.0
130819 31 II	2	no	3.8	1.4	2.4	0.58	9.1
130807 20 I	3	yes	4.2	1.8	1.3	1.38	5.5
130819 31 II	3	no	7.0	4.0	2.4	1.67	16.8

## 2. Conductance of All Devices

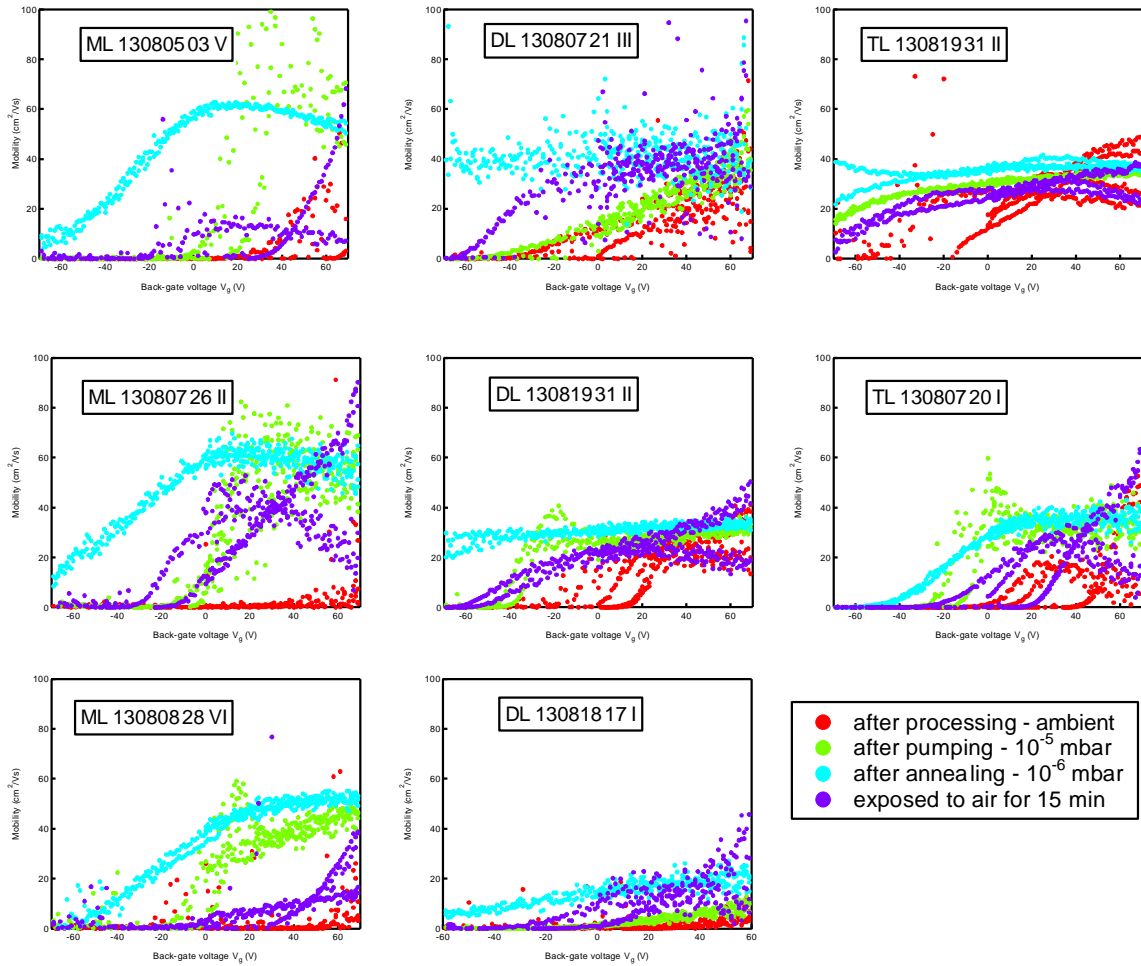
The evolution of four-probe conductance during the process of cleaning and exposing to ambient for all characterized devices as listed in Section 1.



**Figure SI 1. Evolution of four-probe conductance during the process of cleaning and exposing to ambient.** The four shown steps are: right after fabrication in ambient (red), in vacuum ( $\sim 1 \times 10^{-5}$  mbar) before overnight annealing (green), in vacuum ( $\sim 1 \times 10^{-6}$  mbar) after overnight annealing (blue) at  $120^\circ\text{C}$  and after  $\sim 15$  minutes of exposure to ambient (purple).

### 3. Mobility of All Devices

The evolution of mobility during the process of cleaning and exposing to ambient for all characterized devices as listed in Section 1.



**Figure SI 2. Evolution of mobility during the process of cleaning and exposing to ambient.** The four shown steps are: right after fabrication in ambient (red), in vacuum ( $\sim 1 \times 10^{-5}$  mbar) before overnight annealing (green), in vacuum ( $\sim 1 \times 10^{-6}$  mbar) after overnight annealing (blue) at 120 °C and after  $\sim 15$  minutes of exposure to ambient (purple).

#### 4. Student t-Test

We perform a statistical t-test and formulate our null-hypothesis as: “The band mobility in monolayer devices is lower than in devices based on two and three layer thick MoS<sub>2</sub>“. The test is based on the following statistics:

Label	#	$\mu_{\text{band}} [\text{cm}^2 \cdot \text{V}^{-1} \text{s}^{-1}]$
130805 03 V	1	62.7
130807 26 II	1	61.2
130808 28 VI	1	52.8
130807 21 III	2	43.5
130818 17 I	2	19.6
130819 31 II	2	32.1
130807 20 I	3	35.4
130819 31 II	3	36.9

We deduce a mean value  $\bar{x}_1$  of  $58.9 \text{ cm}^2 \cdot \text{V}^{-1} \text{s}^{-1}$  for the monolayer FETs and  $\bar{x}_2$  of  $33.5 \text{ cm}^2 \cdot \text{V}^{-1} \text{s}^{-1}$  for FETs based on thicker layers. The standard deviations of our sample sets are  $\bar{s}_1 = 5.4 \text{ cm}^2 \cdot \text{V}^{-1} \text{s}^{-1}$  and  $\bar{s}_2 = 8.8 \text{ cm}^2 \cdot \text{V}^{-1} \text{s}^{-1}$ , respectively. The t-value is given by

$$t = \frac{\bar{x}_1 - \bar{x}_2}{\sqrt{\frac{s_1^2}{N_1} + \frac{s_2^2}{N_2}}}$$

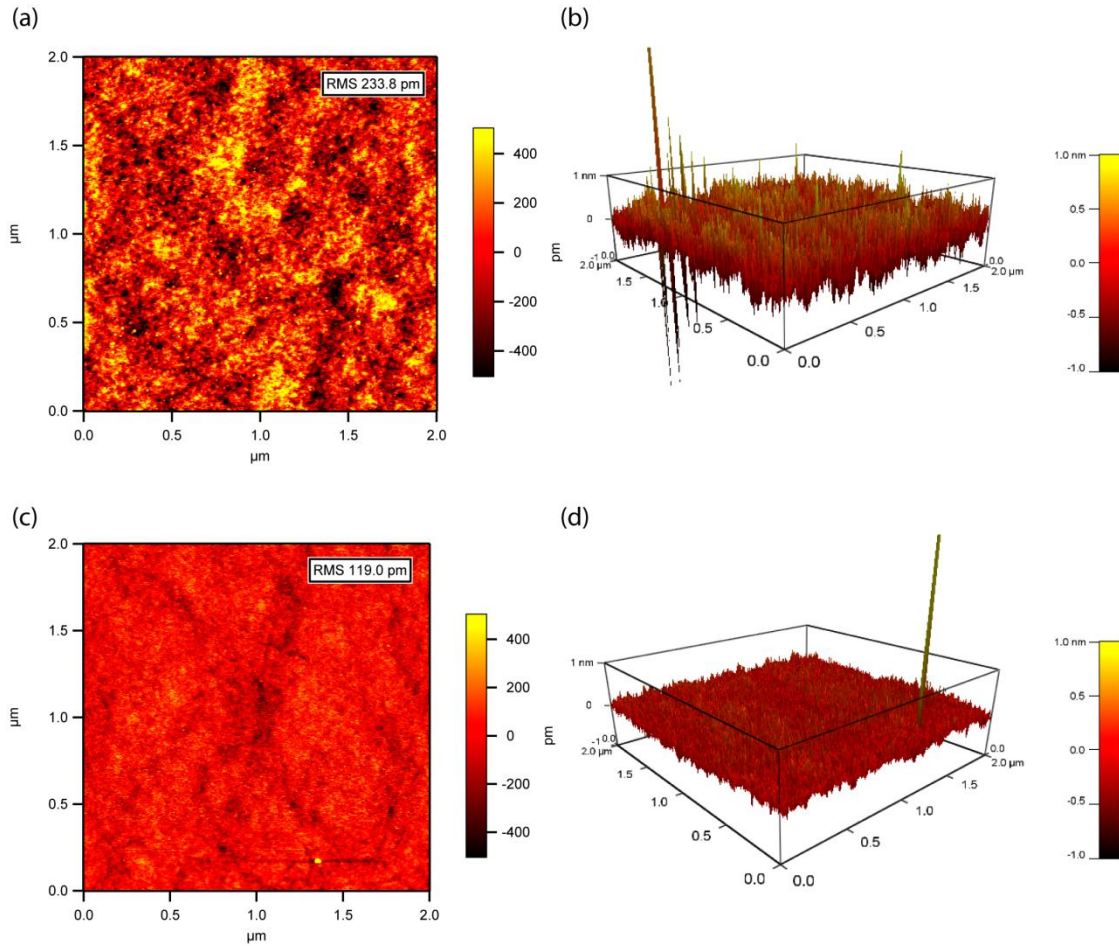
The degree of freedom d.f. of this test is given by the Welch–Satterthwaite equation

$$d.f. = \frac{\left(\frac{s_1^2}{N_1} + \frac{s_2^2}{N_2}\right)^2}{\frac{\left(\frac{s_1^2}{N_1}\right)^2}{N_1-1} + \frac{\left(\frac{s_2^2}{N_2}\right)^2}{N_2-1}}$$

With this, we calculate a t-value of 5.1 and a d.f. of 5.9. By comparing these values with the theoretical z-score we can reject our initial hypothesis that the monolayer device has a lower mobility than thicker ones with a probability of error of less than 0.5%. In other words, we can say that the mobility of our monolayer MoS<sub>2</sub> devices is higher than the other devices with a confidence of at least 99.5%.

## 5. Ultra-flat SiO<sub>2</sub> Substrate

The SiO<sub>2</sub> substrate of ~half of the devices was intentionally chemically and mechanically polished by using a commercial CMP machine (Alpsitec E460) to establish an ultra-flat substrate prior to exfoliation. The polishing of SiO<sub>2</sub> results in an ultra-smooth substrate and the RMS value of the surface height can be reduced from a value of 230 pm in the unpolished SiO<sub>2</sub> to 119 pm in the polished surface.



**Figure SI 3. Morphology of the SiO<sub>2</sub> substrate.** (a) AFM image ( $2 \times 2 \mu\text{m}^2$ ) of the unpolished SiO<sub>2</sub> surface. The RMS of this surface is 233.8 pm. (b) 3D representation of the image in (a). (c) AFM image ( $2 \times 2 \mu\text{m}^2$ ) of the polished SiO<sub>2</sub> surface after CMP treatment, exhibiting a RMS of 119.0 pm. (d) 3D representation of the image in (c).