Electronic Supplementary Material (ESI) for Nanoscale.
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Electronic Supplementary Information for:

Trap density probing on top-gate MoS_2 nanosheet field-effect transistors by photo-excited charge collection spectroscopy

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ESI 1.

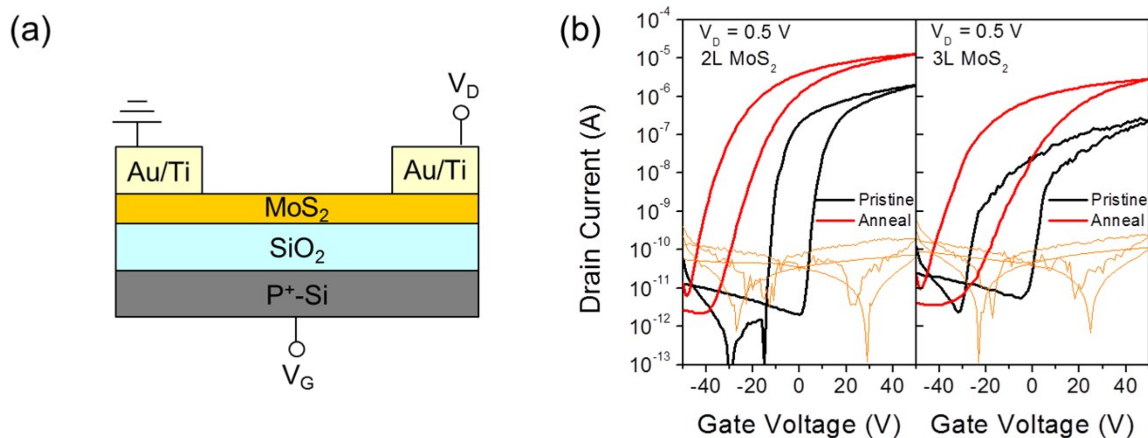

Fig. S1 (a) The 2D schematic of the universal back-gate MoS_2 FET. (b) Transfer curves of 2L and 3L MoS_2 FETs before and after thermal annealing. After patterning of Source (S) and drain (D) electrodes, thermal annealing was carried out at 473K for 10 min in a N_2 atmosphere. A negative shift of threshold voltage in universal back-gate FETs was always found after the annealing, as indicated in the transfer curves of Fig. S1b.

ESI 2.

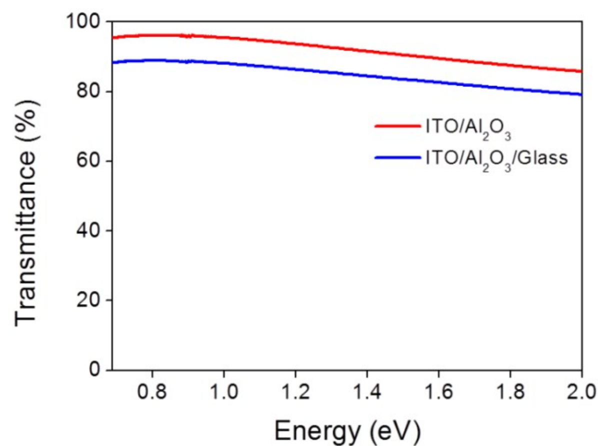

Fig. S2 The transmittance of the ITO/Al_2O_3 and ITO/Al_2O_3/glass samples was more than 80%.

ESI 3.

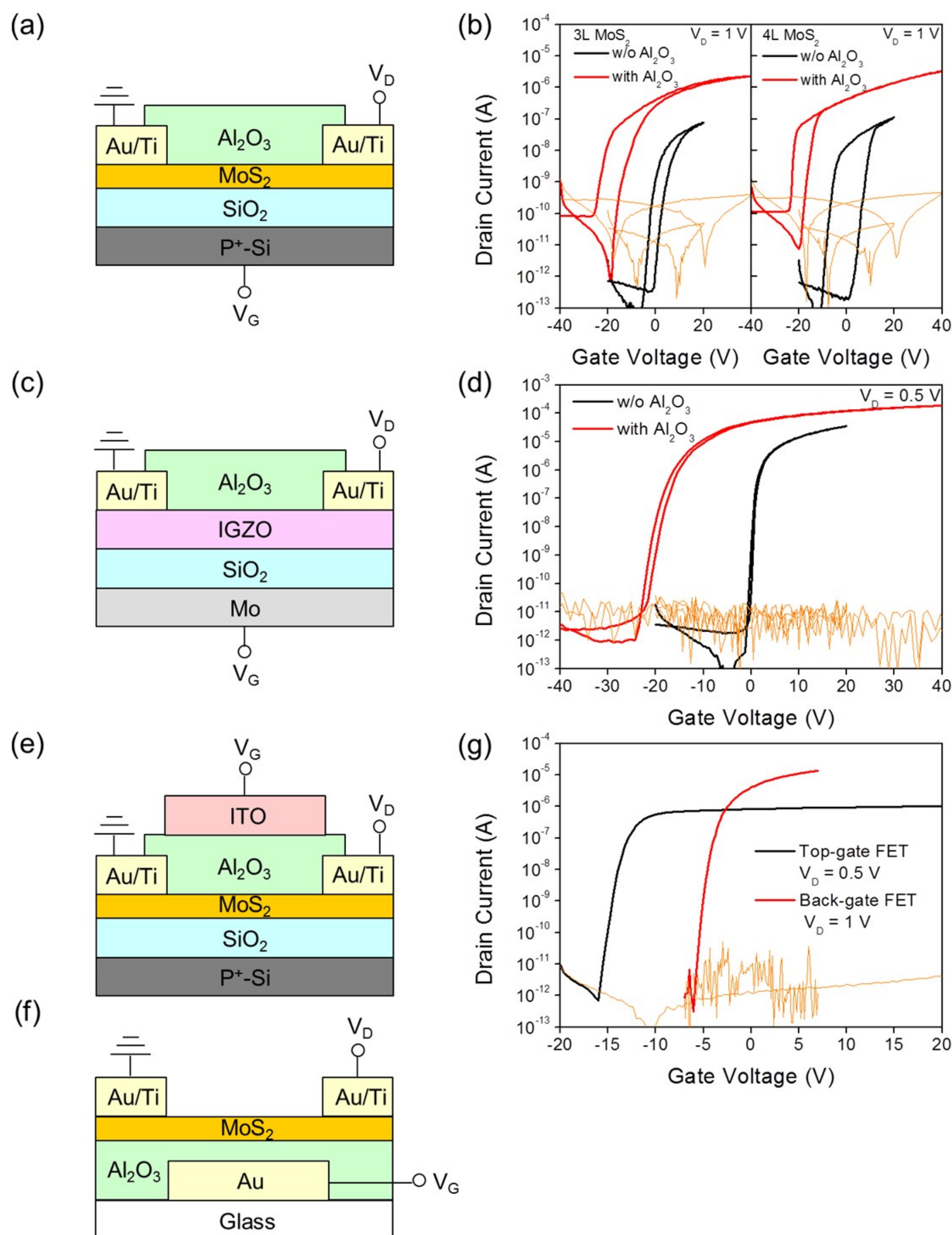

Fig. S3 (a,b) Device schematics and transfer curves of universal back-gate 3-4 L MoS_2 channel FETs with and without 50 nm-thick ALD Al_2O_3 passivation. (c,d) Device schematics and transfer curves of universal back-gate n-type InGaZnO channel FETs with and without 50 nm-thick ALD Al_2O_3 passivation. (e~g) Device schematics of top-gate (e) and patterned back-gate (f) MoS_2 FETs along with their respective transfer curves.

According to the transfer curves of Fig. S3b and d, there is big difference between two universal back-gate FETs with and without ALD Al_2O_3 encapsulation. A large increase of drain current and threshold voltage shift is observed by simple ALD encapsulation. This indicates that carrier doping effects from ALD oxide to channel are highly likely, making the channels more conductive than before ALD process. Transfer curves of Fig. S3g show the results from patterned back-gate MoS_2 FET, where exfoliated MoS_2 was printed on Al_2O_3 dielectric that was already deposited by ALD; no doping effects are expected. The threshold voltage of back-gate MoS_2 FET appeared quite smaller than that of top-gate FET. This result evidences that the large negative threshold voltage issue comes from the ALD-induced doping.

ESI 4.

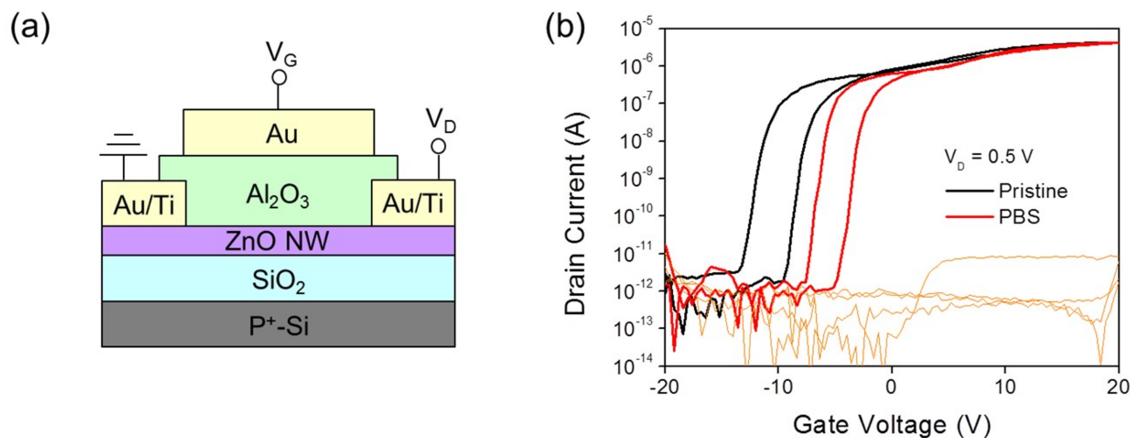

Fig. S4 (a) Device schematic of top-gate ZnO nanowire FET. (b) The transfer curves of top-gate ZnO nanowire FET before (Pristine) and after 1000 s-period positive gate bias stress (PBS) under V_G=20V and V_D=0.5 V. Single-crystalline ZnO nanowire-based FETs with ALD Al_2O_3 dielectric was subjected to positive bias stress (PBS) under the conditions of V_G=20 V and V_D=0.5 V for 1000s. According to the curves, the transfer curve and threshold voltage significantly shift to the positive side after the PBS. It is due to defective ZnO nanowire surface, not because of Al_2O_3 quality. It means that our MoS_2 surface is quite clean and our ALD Al_2O_3 itself is OK in its quality. We regard that only a main problem is ALD process which introduces dopants and impurities to the bulk MoS_2.

ESI 5.

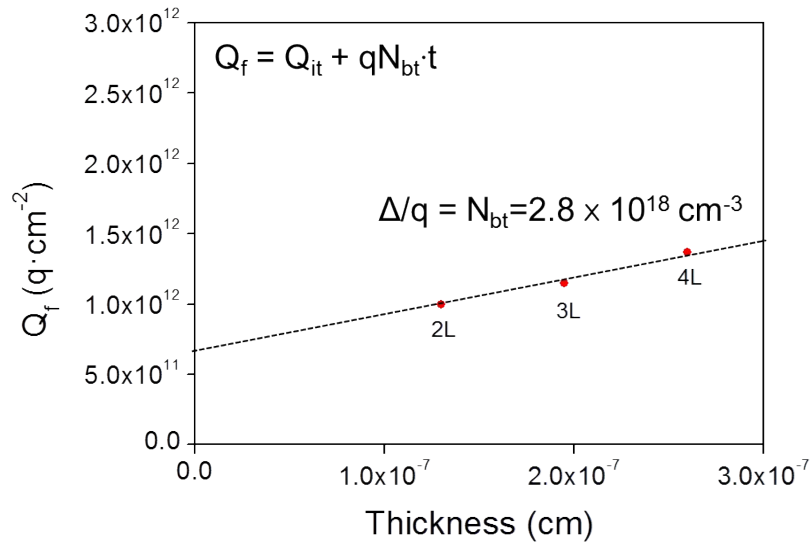

Fig. S5 Thickness (t)-dependent Q_f plots from 2L, 3L and 4L MoS_2 FETs. We extracted out the Q_{it} and N_{bt} values as 0.7×10^{12} q·cm^{-2} and 2.8×10^{18} cm^{-3}, respectively, based on the t-dependent Q_f plots as above. The plot has been made according to $|\Delta Q_{eff}(\varepsilon)|$ data for 2L, 3L, 4L as indicated by arrows in Fig. 4(d)

ESI 6.

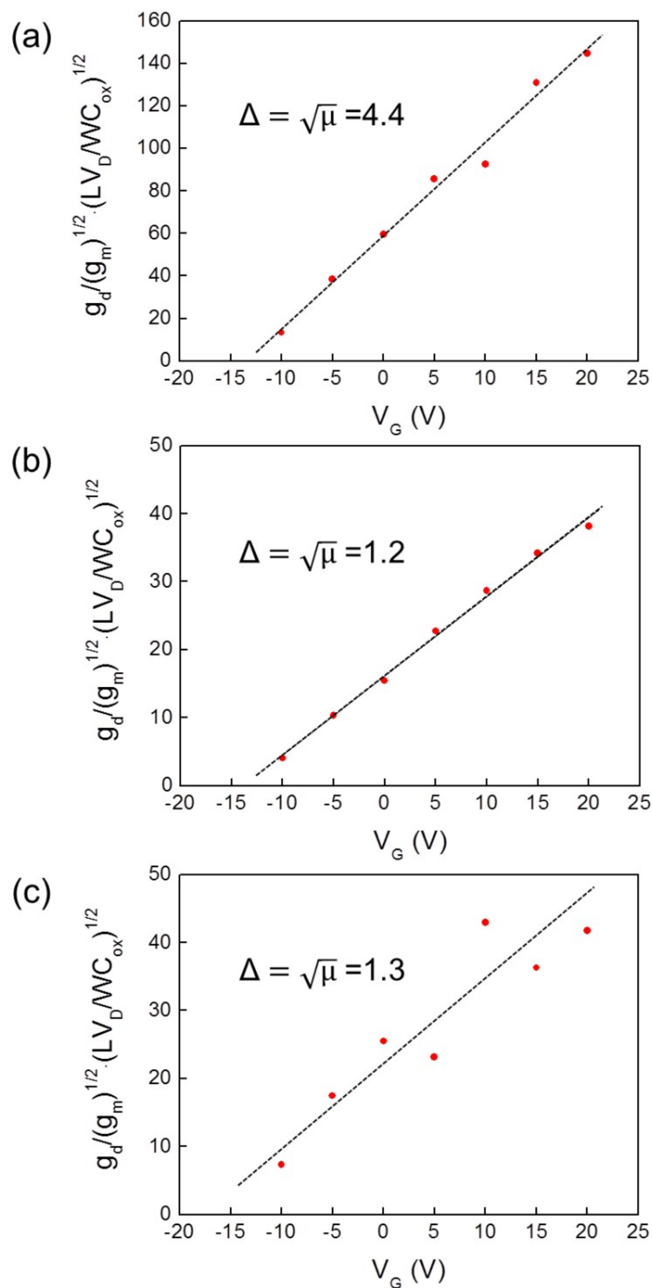

Fig. S6 Slop of the curve indicates the square root of mobility ($\sqrt{\mu}$) for the (a) 2L, (b) 3L, and (c) 4L MoS_2 FETs after removing the contact resistance. So, μ is 19.4, 1.44, and 1.7 $cm^2/V{\cdot}s$ for 2L, 3L, and 4L MoS_2 FETs, respectively.

At low drain voltage (V_D), the drain current (I_D) is depicted by Eqn (1)

$$I_D = \frac{W}{L} C_{ox} \mu (V_G - V_{Th}) V_D \tag{1}$$

where W/L is width/length ratio, C_{ox} is dielectric capacitance per unit area, and V_{Th} is threshold voltage. Adding the voltage drop through a contact resistance (R_C) in Eqn (1) will end up with Eqn (2)[1]

$$I_D = \frac{W}{L} C_{ox} \mu \left(V_G - V_{Th}\right)\left(V_D - I_D R_C\right) \tag{2}$$

$$= \frac{(W/L) C_{ox} \mu (V_G - V_{Th}) V_D}{1 + (W/L) C_{ox} \mu R_C (V_G - V_{Th})}$$

The drain conductance (g_d) and transconductance (g_m) can be estimated by Eqn (3) and (4), respectively.

$$g_d = \frac{\partial I_D}{\partial V_D} = \frac{(W/L) C_{ox} \mu (V_G - V_{Th})}{1 + (W/L) C_{ox} \mu R_C (V_G - V_{Th})} \tag{3}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{(W/L) C_{ox} \mu V_D}{[1 + (W/L) C_{ox} \mu R_C \left(V_G - V_{Th}\right)]^2} \tag{4}$$

To eliminate the R_C, we divide Eqn (3) by the square root of Eqn (4), and finally we could obtain Eqn (5)

$$\frac{g_d}{\sqrt{g_m}} \sqrt{\frac{L\, V_D}{W C_{ox}}} = \sqrt{\mu} (V_G - V_{Th}) \tag{5}$$

Using Eqn (5), we can extract out the channel mobility without contact resistance; measuring (g_d) and (g_m) from real transfer and output curves, we can plot $\frac{g_d}{\sqrt{g_m}}\sqrt{\frac{L\,V_D}{WC_{ox}}}$ vs. (V_G) curves for each FET at a constant small V_D. Since (g_d) and (g_m) are functions of V_G according to respective Eqn (3) and (4), $\frac{g_d}{\sqrt{g_m}}\sqrt{\frac{L\,V_D}{WC_{ox}}}$ should a function of V_G, too. The plot must be linear and the respective slope would be $\sqrt{\mu}$. Now the mobility is estimated in this way, to be 19.4, 1.44, 1.7 $cm^2/V{\cdot}s$ for 2L, 3L, and 4L MoS_2 FET, respectively. The linear channel mobilities are almost the same as the peak linear mobilities in 3L and 4L MoS_2 FETs, while it is 7 times larger than that of 2L MoS_2 FET. It is probably because 2L MoS_2 has larger band gap and schottky barrier as well.

Reference

Ref. S1 G. Horowitz, R. Hajlaoui, D. Fichou, A. E. Kassmi, *Appl. Phys. Lett.*, 1999, **85**, 3202.