Electronic Supplementary Material (ESI) for RSC Advances

Supplementary information: Printed conductive features for DNA chip applications prepared on PET without sintering

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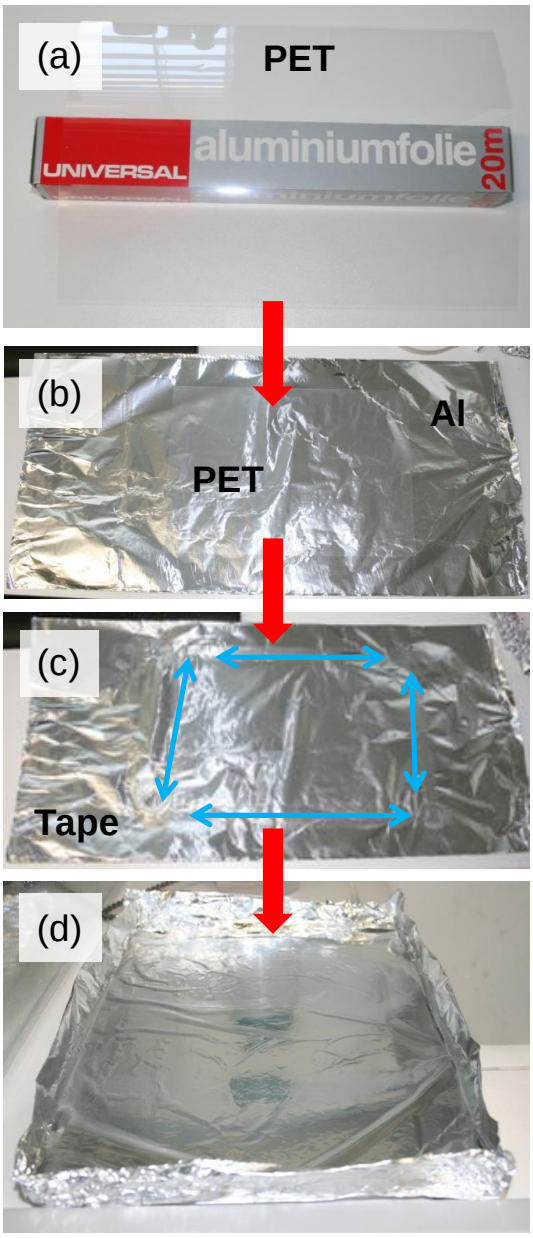
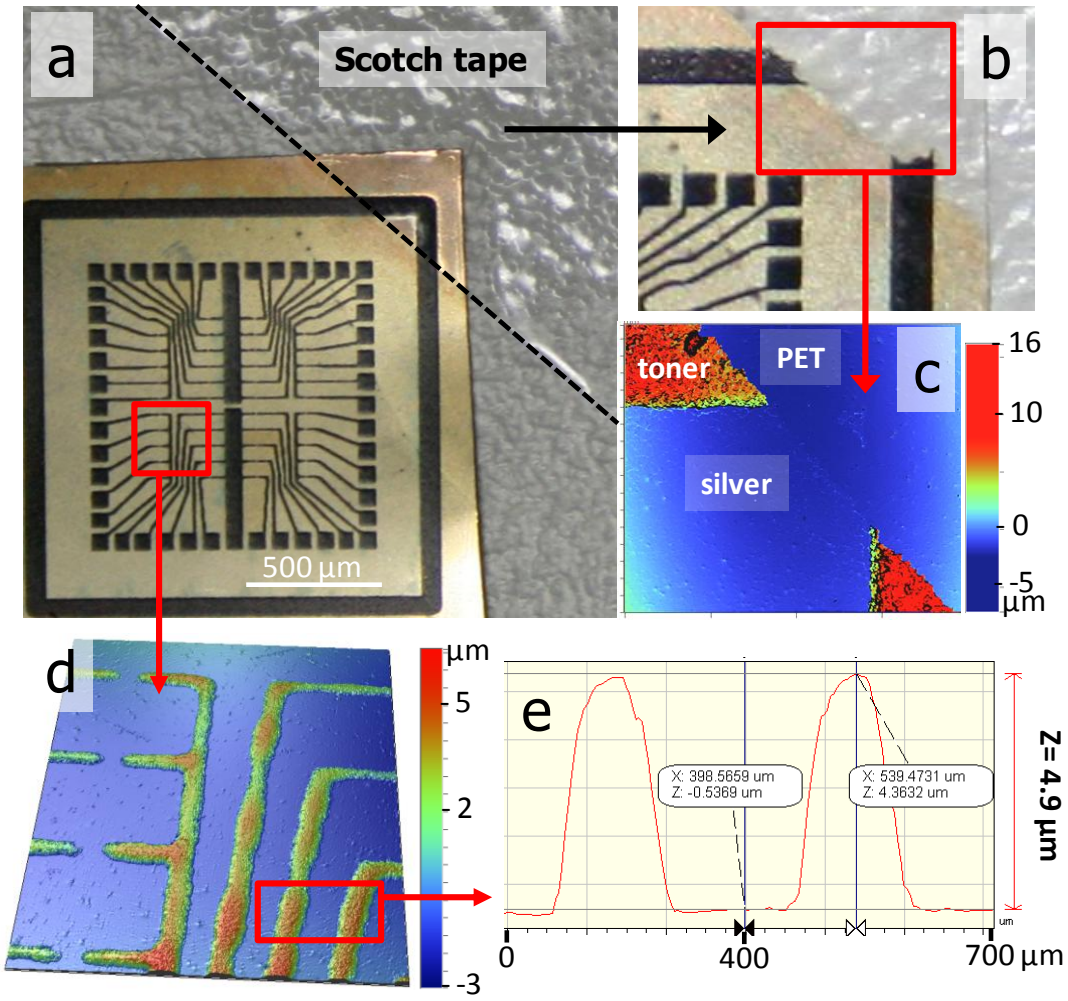
Sample preparation

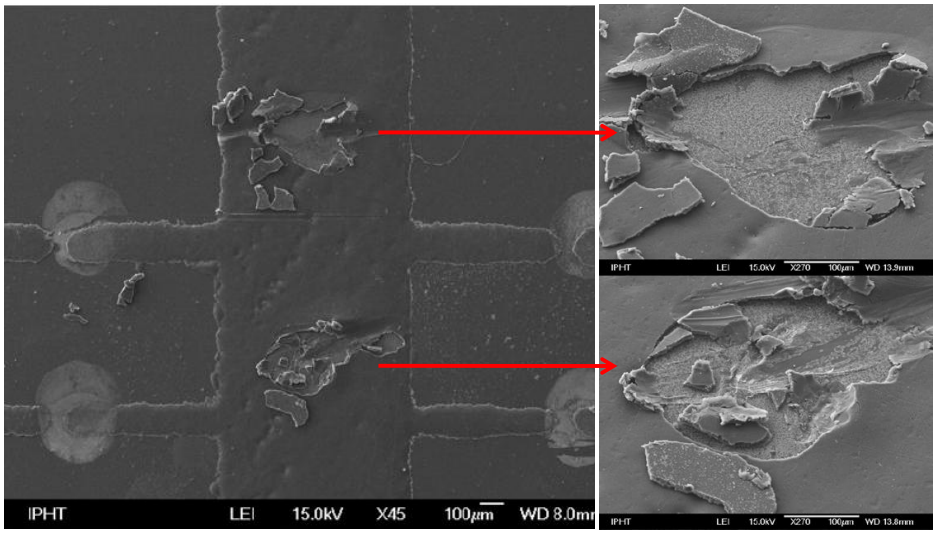


Supplementary Information Figure 1. Preparation of the PET substrate for silver deposition: (**a**) materials that are needed, (**b**) placement of the PET foil on the aluminum foil, (**c**) sealing of the PET by using scotch tape, (**d**) bending of the edges of the aluminum foil upwards to prevent leaking of liquid.

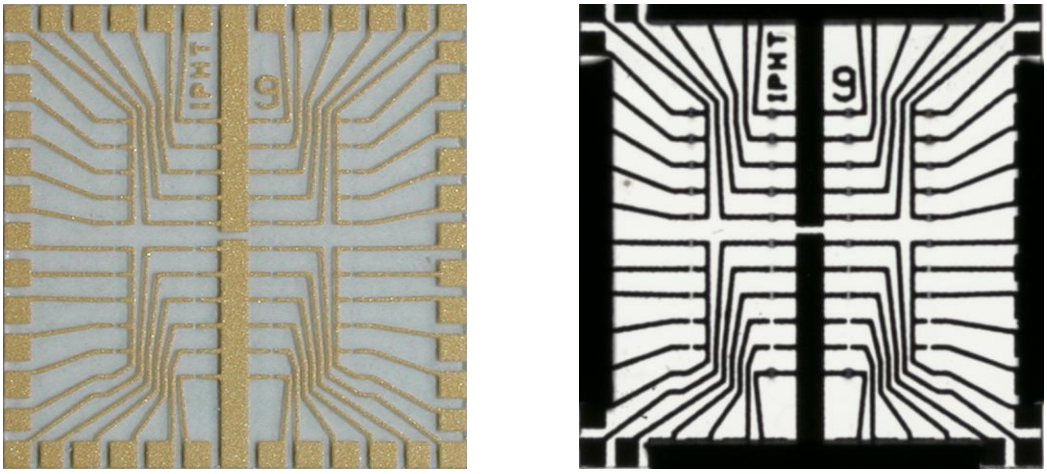
Circuit board patterns analysis



Supplementary Information Figure 2. Circuit board pattern analyses before and after partial removal by scotch tape. (**a**) Circuitry pattern prepared and scotch tape attached on the top right corner, (**b**) after removal of the scotch tape, the uncoated PET layer is visual. Confocal interferometry analysis of (**c**) silver and toner thickness, (**d**) patterns profiles and (**e**) height measurements.



Supplementary Information Figure 3. Printed circuit board after using in a DNA Chip reader: the pins of the DNA reader easily brake through the black toner material in order to reach the layer of silver, as shown on the images on the right hand side.



Supplementary Information Figure 4. For comparison to the printed chips, screen-printed gold microelectrode structures on glass with DNA detection (left) and optical readout (right) by scanning the sample in black and white. The length and width of a chip is 2.54 cm.

Calculation of circuit board fabrication expenses

When the chips are produced in the clean room at the IPHT (Jena, Germany), the cost per chip are approximately € 20 to € 30, depending on the size and layout of the chip. When producing the chips at larger scale and on 6- or 8-inch wafers, the costs could be reduced to € 5 to € 10 per

chip. The screen printed glass chips that we use now cost € 1 to € 2.50 per chip when we order them from Heraeus. The disadvantage of both fabrication methods is, besides the price, that small changes in the layout always need new masks, which increases the overall costs significantly. Both methods result in lower price per chips if produced in larger volumes. Therefore, the methods are not useful for "rapid prototyping" or to test new layouts.

In contrast to the above mentioned prices, the typical cost for the method presented here was € 5000 per 1000 identical items, which is the number of replications and a lower limit for the manufacturer. In comparison, our method can deliver a single item as well as a thousand of them, while keeping the same costs per item. Scaling-up or down is, therefore, vey cost effective. Our calculations indicate that for preparing 110 chips, which was sufficient to test the DNA chips, the costs were less than € 0.10 per chip.