Electronic Supplementary Material (ESI) for RSC Advances.


# Supplementary Information to "Flexible One Diode-One Resistor Resistive Switching Memory Arrays on Plastic Substrates"

Hyeon Gyun Yoo, Seungjun Kim, and Keon Jae Lee*

Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST) 291 Daehak-ro, Yuseong-gu, Daejeon 305-701 (Republic of Korea)

E-mail: keonlee@kaist.ac.kr

## 1. Device fabrication process

Fig. S1 shows schematics of the fabrication steps for flexible 1D-1R RRAM on a plastic substrate. Patterned silicon nanomembranes were transferred from a silicon on insulator (SOI) wafer onto a polyimide substrate (DuPont, Kapton) with a spin-cast PI precursor (Poly(amic aci(d), Sigma Aldrich) as an adhesive.[1,2] After transfer process, active regions (300 × 150 $\mu m^2$) of diodes were isolated by photolithography and $SF_6$ plasma etching. The PI precursor was fully cured at 250 °C for 1h in a nitrogen atmosphere [Fig. S1a]. The layers of Au/Cr (200 nm/10 nm) for metal contacts and Cu/Cr (250 nm/10 nm) for bottom electrodes were deposited respectively on anode and cathode regions of diodes using a radio-frequency (RF) sputtering and lift-off process [Fig. S1b]. Copper oxide layers were formed by plasma oxidation process in an inductively coupled plasma-reactive ion etching (ICP-RIE) system with RF power of 200 W for 10 min at room temperature [Fig. S1c]. After formation of the copper oxide layer, the Al top electrodes were formed in the same way as the bottom electrodes [Fig. S1d]. The bit lines and word lines of Au/Cr (200 nm/10 nm) were patterned sequentially through a radio-frequency (RF) sputtering and wet etching. Spin-cast SU-8 layer with photo-lithographically opened interconnect access holes were employed as the interlayer dielectric between the metal layers. [Fig. S1e and S1f].

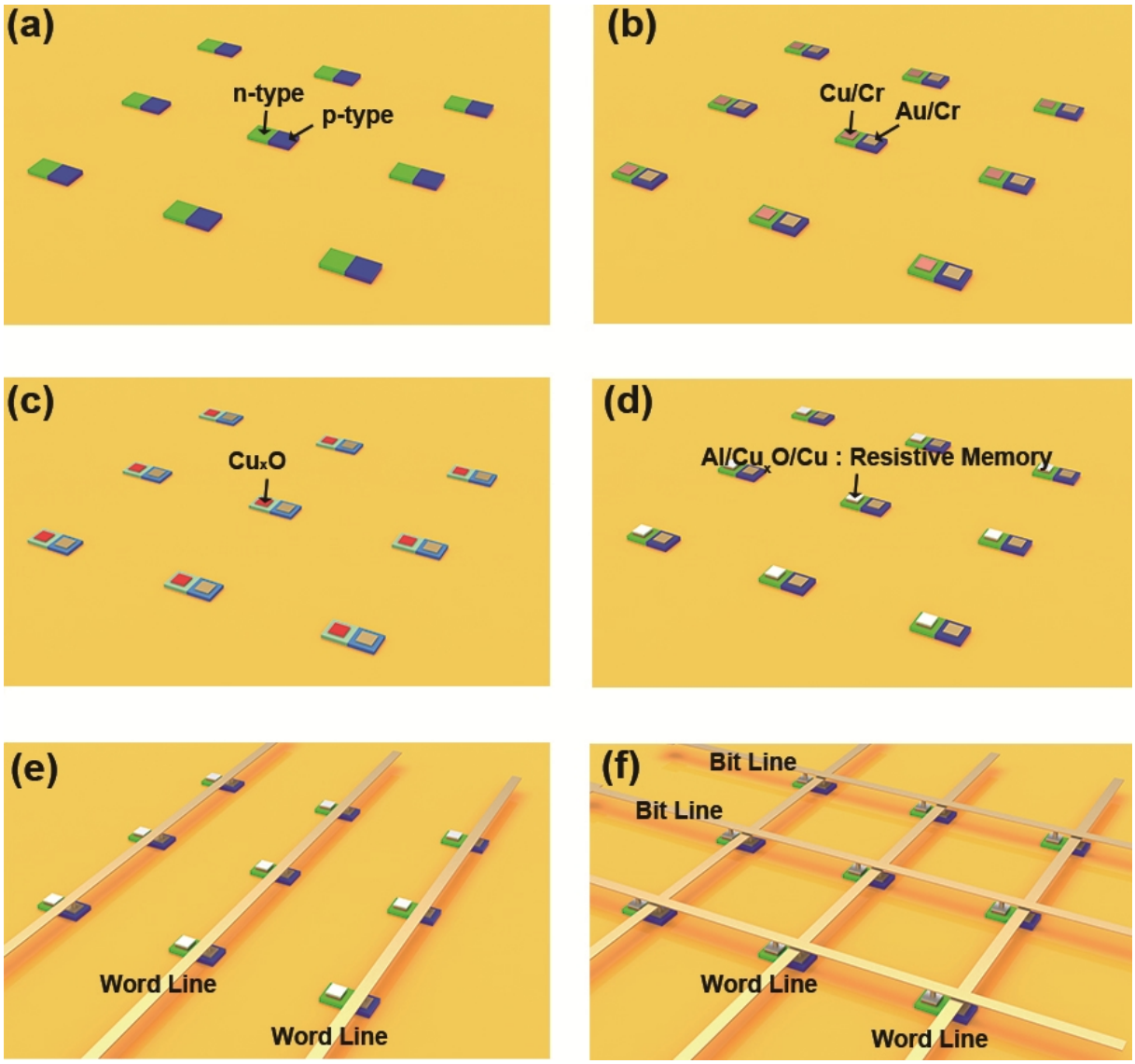


**Fig. S1.** Detail schematic illustration of the process for fabricating 1D-1R RRAM on a plastic substrate. (a) Transfer-printing of silicon nanomembrane onto a polyimide substrate. (b) Deposition of metal layers (c) Plasma oxidation for forming copper oxide layer. (d) Deposition of Al top electrodes. (e-f) Interconnection of memory cells through word and bit lines.

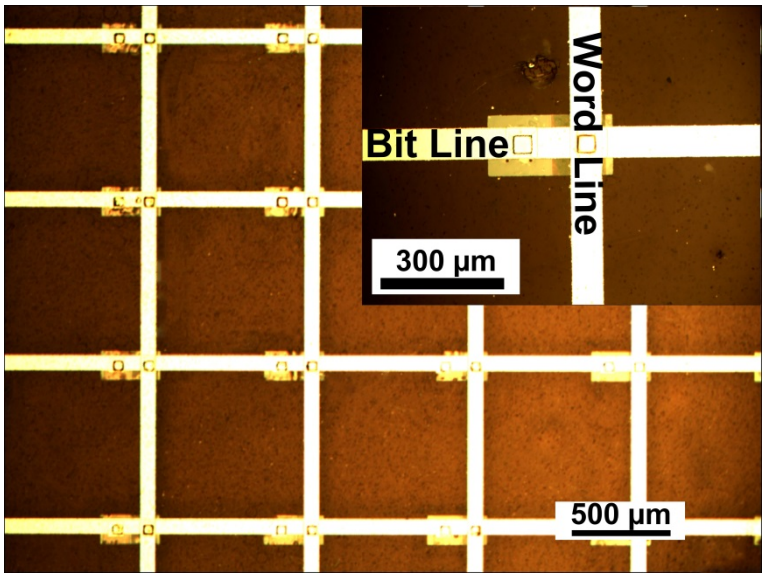


**Fig. S2.** A magnified optical image of the flexible 1D-1R device. The inset shows 1D-1R unit cell in memory array. The active area of the diode and resistive memory are 300 × 150 $\mu m^2$ and 50 × 50 $\mu m^2$, respectively.

**2. The forming process of flexible RRAM.**

Fig. S3a-b shows the I-V properties of a forming, RESET, and SET processes of 1R and 1D-1R memory. As shown in Fig. S3a-b, the forming processes are observed at 3.6 V for 1R and 3.8 V for 1D-1R, respectively. After the forming process, the developed device shows reproducible resistive switching characteristics.

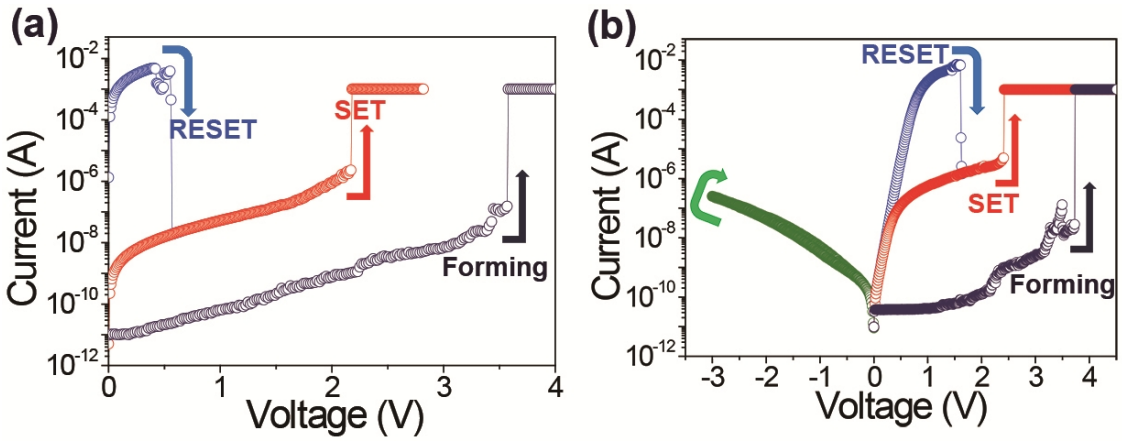


**Fig. S3.** (a) The I-V curves of the 1R RRAM. The forming voltage is 3.6 V. (b) The I-V curves of the 1D-1R RRAM. The forming voltage is 3.8 V.

**3. The DC I-V curves of flexible 1D-1R memory & Statistical analysis of flexible silicon diode**

Fig. S4a shows the cumulative probability data of both the forward and reverse state resistance at ±1 V measured by I-V curves of 40 silicon diodes. The inset of Fig. S4a shows the rectifying ratio distribution depicted by a box-whisker plot obtained from the I-V curves of 40 silicon diodes. Fig. S4b shows the switching I-V curves of the 1D-1R memory cell. During the SET operation in dc voltage sweep mode, a compliance current of 1 mA was selected to avoid the permanent breakdown of 1D-1R device. This result presents that the flexible 1D-1R memory exhibits stable resistive switching cycles. The inset of Fig. S4b shows the SET and RESET voltage distribution of the flexible 1D-1R memory cell depicted by a box-whisker plot obtained from the I-V curves of 50 switching cycles.

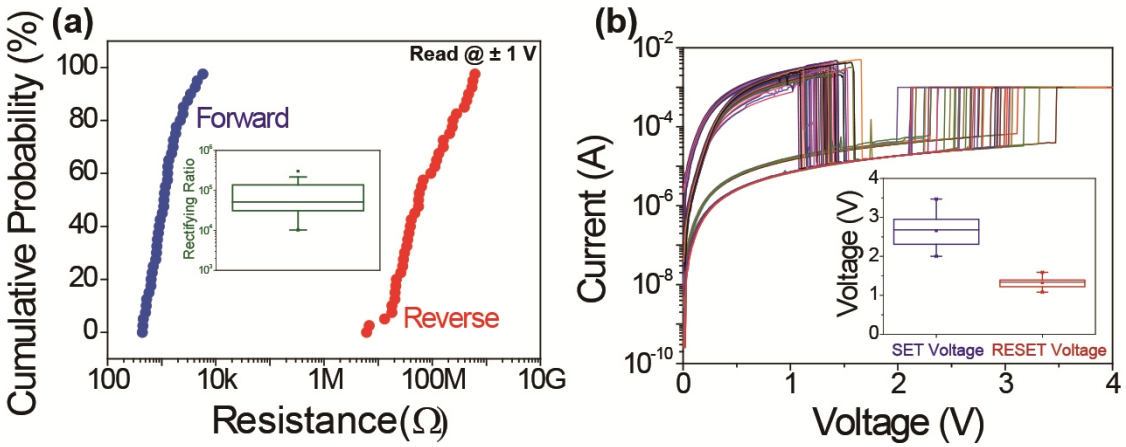


**Fig. S4.** (a) The statistical characteristics of silicon diodes. The inset shows the rectifying ratio distribution of silicon diodes (b) The DC I-V curves of the flexible 1D-1R RRAM in forward bias region. The inset presents the SET and RESET voltage distributions of flexible 1D-1R memory cell.

**4. Statistical analysis of flexible 1D-1R memory**

Fig. S5a shows the cumulative probability data of both the LRS and HRS measured by I-V curves of 55 memory cells. The LRS exhibits narrow distribution, but distribution of the HRS shows broad distribution, which may be related to the variation of the ruptured filament path length.[3] Fig. S5b shows the current density-voltage characteristics of the silicon diode in the forward bias. The silicon diode provides the sufficient current density ($>10^5$ A/cm$^2$) to operate unipolar resistive memory. The inset of Fig. S5b shows the forward state resistance of the silicon diode according to the applied voltages. This result shows non-linear behavior of resistance state in forward bias, and this non-linearity plays a significant role as a buffer resistor enhancing programming margin of the 1D-1R device. Fig. S5c shows the SET and RESET voltage distribution of the flexible 1D-1R RRAM depicted by a box-whisker plot obtained from I-V curves of 55 memory cells. When compared with voltage distribution of 1R memory cell without selection diodes in the inset of Fig. S5c, it is found that the programming voltage margin between the SET and RESET is greatly stabilized by integrating selection diodes. This result shows that the silicon diode plays important roles of a selection device to prevent cell-to-cell interference as well as a buffer resistor to suppress excessive current flow during SET process.[4,5] Fig. S5d shows the retention characteristics of flexible 1D-1R device measured at 80 °C, demonstrating that no significant change of the resistance occurs in both the LRS and HRS for $10^4$ s.

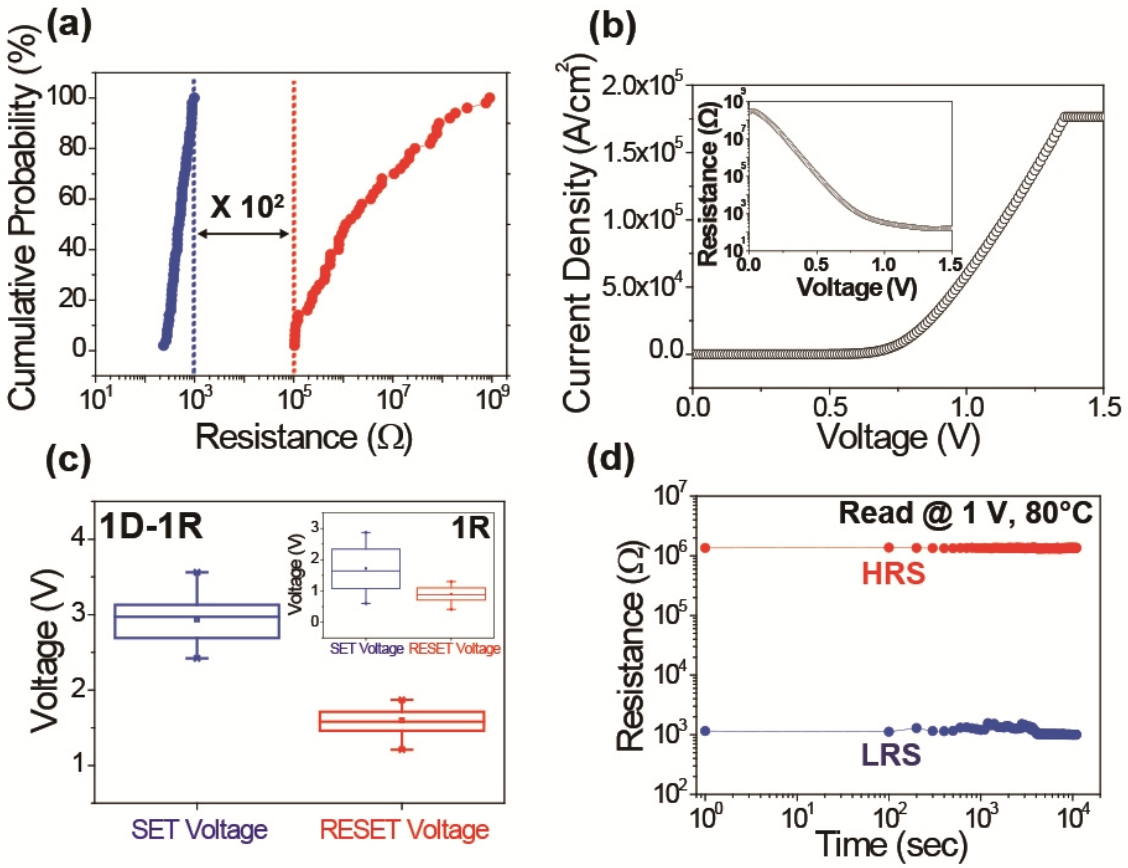


**Fig. S5.** (a) Cumulative probability data of each the HRS and LRS obtained from I-V curves of 55 unit cells. (b) Current density-voltage characteristics of a silicon diode under the forward bias. The inset presents the forward state resistance of the silicon diode according to the applied voltages. (c) SET and RESET voltage distributions of the 1D-1R RRAM depicted by a box-whisker plot obtained from I-V curves of 55 unit cells. The inset presents the SET and RESET voltage distributions of 1R memory cells without selection diodes. (d) Retention characteristics of flexible 1D-1R RRAM measured at 80 °C.

**5. Electrical pulse measurement of flexible 1D-1R memory**

The electric pulse measurement of 1D-1R memory was conducted to examine the SET and RESET voltage pulse height and width. 10 switching cycles can be achieved with 500 ns/5 V (SET pulse) and 500 μs/ 2 V (RESET pulse), as shown in Fig. S6. The insets of Fig. S6 present the transition response current waveforms for the SET (left) and RESET processes (right). These results show that the SET and RESET processes are successfully observed at 500 ns and 500 μs of pulse width, respectively.

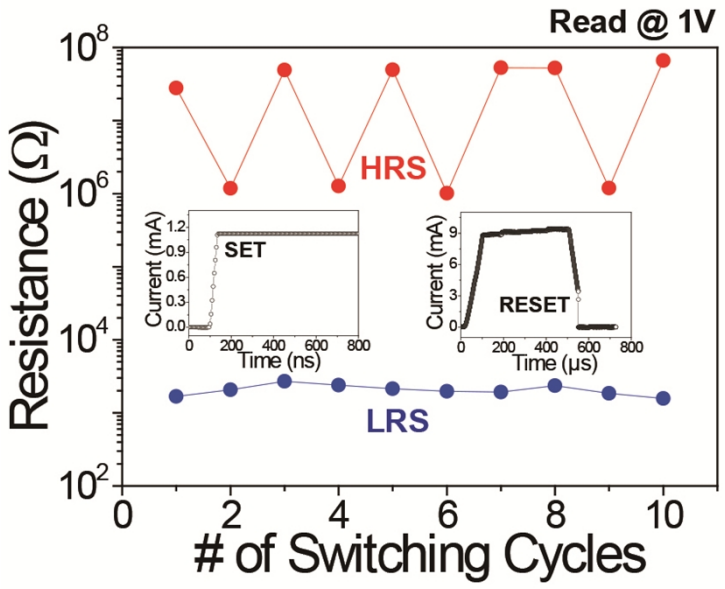


**Fig. S6.** Resistive switching characteristics measured by repeated voltage pulses. The insets show electrical response current waveforms for the SET (left) and RESET (right) processes.

**6. Resistive switching characteristics under the bended condition**

Fig. S7a-b shows the resistive switching characteristics obtained from I-V curves of 10 unit cells as a function of different bending radii and times. As shown in Fig. S7a-b, the 1D-1R device exhibits almost same resistive switching behavior under various bending radii and bending times, which demonstrates that the developed flexible memory has good mechanical stability under the bended condition.

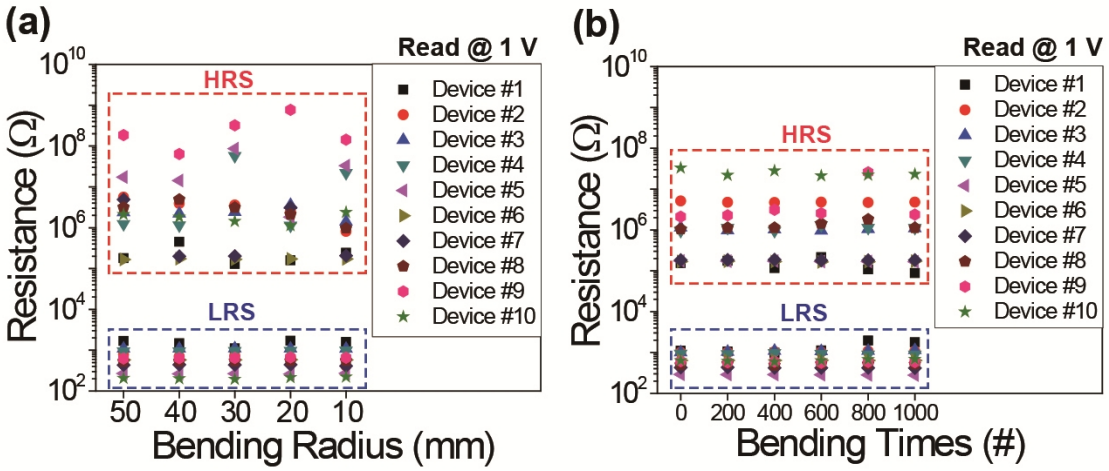


**Fig. S7.** The statistical characteristics of mechanical reliability obtained from I-V curves of 10 unit cells. (a) The resistance values as a function of different radii. (b) The bending fatigue test results.

## 7. Conduction mechanisms of the memory in the LRS and HRS

To further understand the conduction mechanisms of the Al/$Cu_xO$/Cu resistive memory, Fig. S8 shows the double logarithmic plot of I-V characteristics of the Al/$Cu_xO$/Cu resistive memory. The log I-V plot of the LRS clearly shows an Ohmic conduction behavior with a slope of 1, which is originated from the formation of conductive filaments in the copper oxide layer. The log I-V plot of HRS can be divided into three region; Ohmic conduction behavior region ($I \propto V$), square dependence region ($I \propto V^2$), and steep current increasing region ($I \propto V^{8.6}$). This behavior can be explained by trap-controlled space-charge-limited conduction (SCL(C) mechanism that happens in the filament-free region, which is generally indicated by an increasing slope value from Ohm's law ($I \propto V$) to Child's law ($I \propto V^2$), as voltage increases.[6,7]

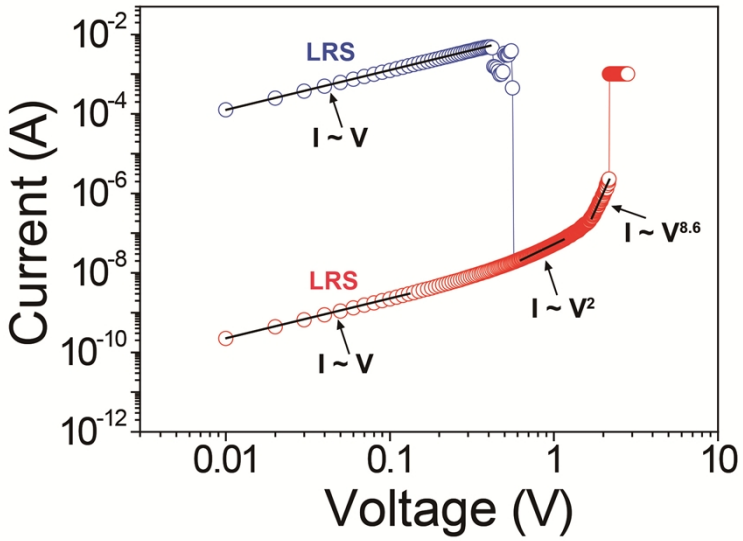


**Fig. S8.** A double-logarithmic plot of the I-V characteristics during the SET and RESET process.

**8. The reading operation for 2 × 2 1R memory cells**

The fabricated $Cu_xO$ RRAM device with 2 × 2 cross-bar structure is shown in Fig. S9. Fig. S10 illustrates the writing process of the 1R memory cells with 2 × 2 array. Before the writing process, the initial state of all memory cells is set to the HRS. Fig. S10a shows that resistance state of the selected (1,1) cell is converted from the HRS to the LRS while other memory cells maintain their original HRS states. Initially, the high resistance state of 869 kΩ of (1,1) cell is read with the reading voltage of 0.1 V. To change the resistance state of (1,1) cell from HRS to LRS, the dc voltage is applied to the selected word and bit lines. After switching the resistance state, the low resistance state of 89 Ω of (1,1) cell is read with the same reading voltage. Similarly, the resistance states of other memory cells are sequentially converted from HRS to LRS in the order of (1,2), (2,1) through the writing process described in the above. After (1,1), (1,2), and (2,1) cells are set to the LRS, the reading voltage is then applied to the (2,2) cell in order to read the resistance value of the (2,2) cell, and the resistance value of (2,2) cell is 148 Ω. From this result, we experimentally measured the cell-to-cell interference occurring through leakage current paths in 1R memory cells without the selection diodes.

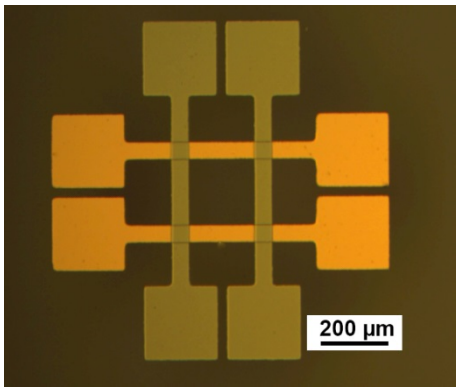


**Fig. S9.** A 2 × 2 cross-bar array $Cu_xO$ RRAM device.

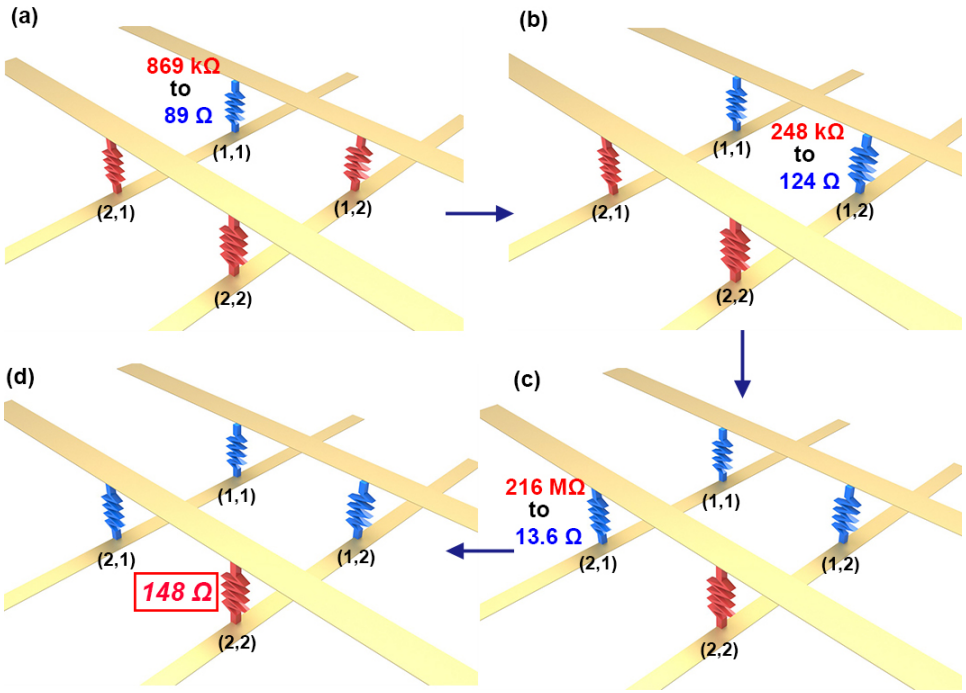


**Fig. S10.** The writing process of 2 × 2 1R memory cells. Red color denotes the HRS (logic state "0") and blue color denotes the LRS (logic state "1").

## 9. The random access operation for 3 × 3 flexible RRAM cells

Fig. S11 shows a schematic of 3 × 3 1D-1R RRAM cells (Fig. S11a and its corresponding circuit diagram (Fig. S11b). The initial state of all memory cells was set to the HRS, represented in red (logic state “0”).

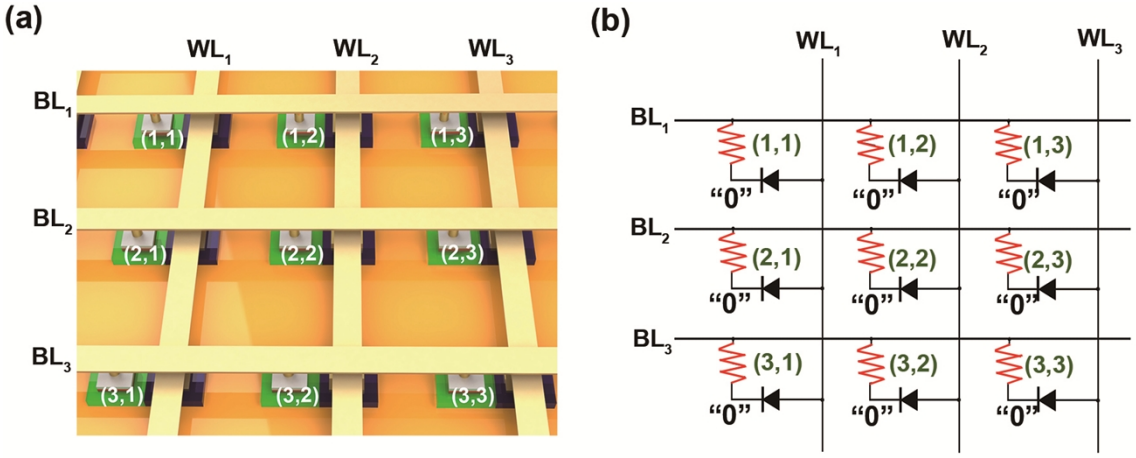


**Fig. S11.** (a) Schematic of 3 × 3 1D-1R RRAM cells. (b) Circuit diagram corresponding to Fig. S11a. Red color denotes the HRS (logic state “0”).

### *A. Writing process*

Fig. S12 illustrates the writing process of the flexible 1D-1R RRAM cells with 3 × 3 array. Fig. S12a shows that resistance state of the selected (1,1) cell is converted from the HRS to the LRS while other memory cells maintain its original HRS state. Initially, the high resistance state of 220 kΩ of (1,1) cell is read with the reading voltage pulse of 5 ms/1 V on a selected word line ($WL_1$). To change the resistance state of (1,1) cell from HRS to LRS, the voltage pulse of 5 ms/5 V (SET pulse) is applied on selected word line ($WL_1$). After switching resistance state, the low resistance state of 0.53 kΩ of (1,1) cell is read with same reading voltage pulse. Similarly, resistance states of other memory cells are sequentially converted from HRS to LRS in the order of (1,2), (1,3), (2,3), (3,3), (3,2), (3,1), (2,1), (2,2) through the writing process described in the above.

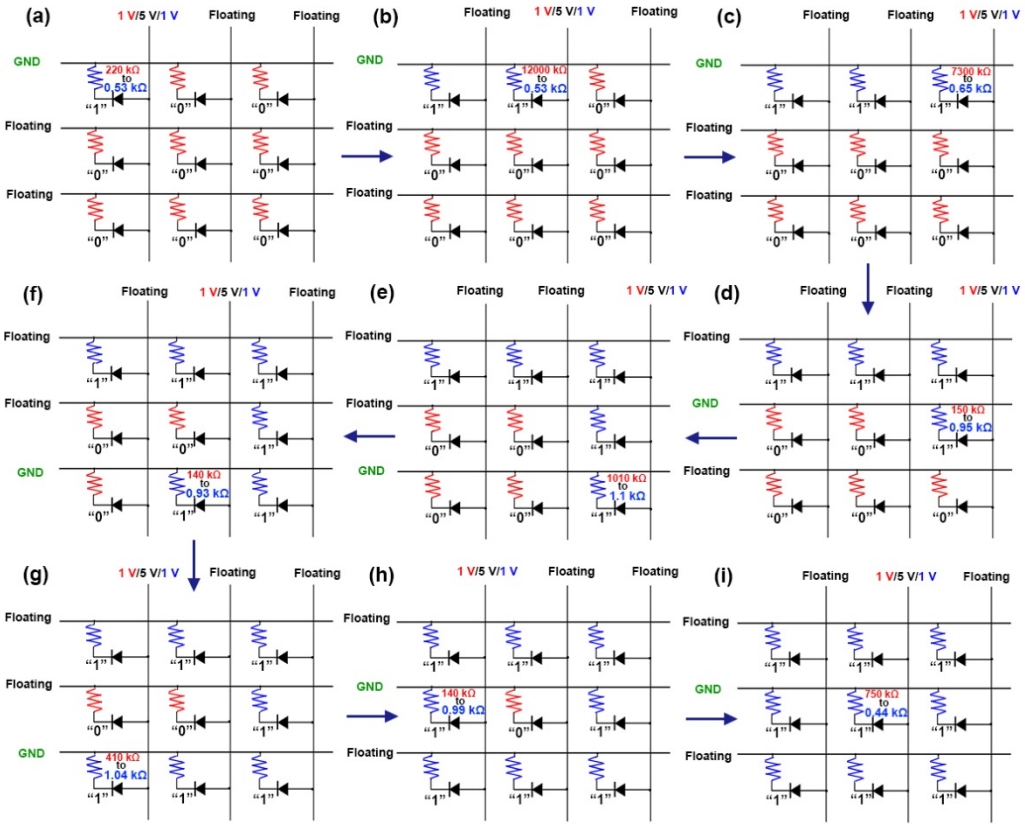


**Fig. S12.** The writing process of 3 × 3 flexible 1D-1R RRAM cells. Red color denotes the HRS (logic state "0") and blue color denotes the LRS (logic state "1").

*B. Erasing process*

Fig. S13 illustrates the erasing process of the flexible 1D-1R RRAM cells with 3 × 3 array. Fig. S13a shows that resistance state of the selected (2,2) cell is converted from the LRS to the HRS while other memory cells maintain its original LRS state. Initially, the low resistance state of 0.44 kΩ of (2,2) cell is read with the reading voltage pulse of 5 ms/1 V on a selected word line ($WL_2$). To change the resistance state of (2,2) cell from LRS to HRS, the voltage pulse of 5 ms/2 V (RESET pulse) is applied on selected word line ($WL_2$). After switching resistance state, the high resistance state of 780 kΩ of (2,2) cell is read with same reading voltage pulse. Similarly, resistance states of other memory cells are sequentially converted from LRS to HRS in the order of (2,1), (3,1), (3,2), (3,3), (2,3), (1,3), (1,2), (1,1) through the erasing process described in the above.

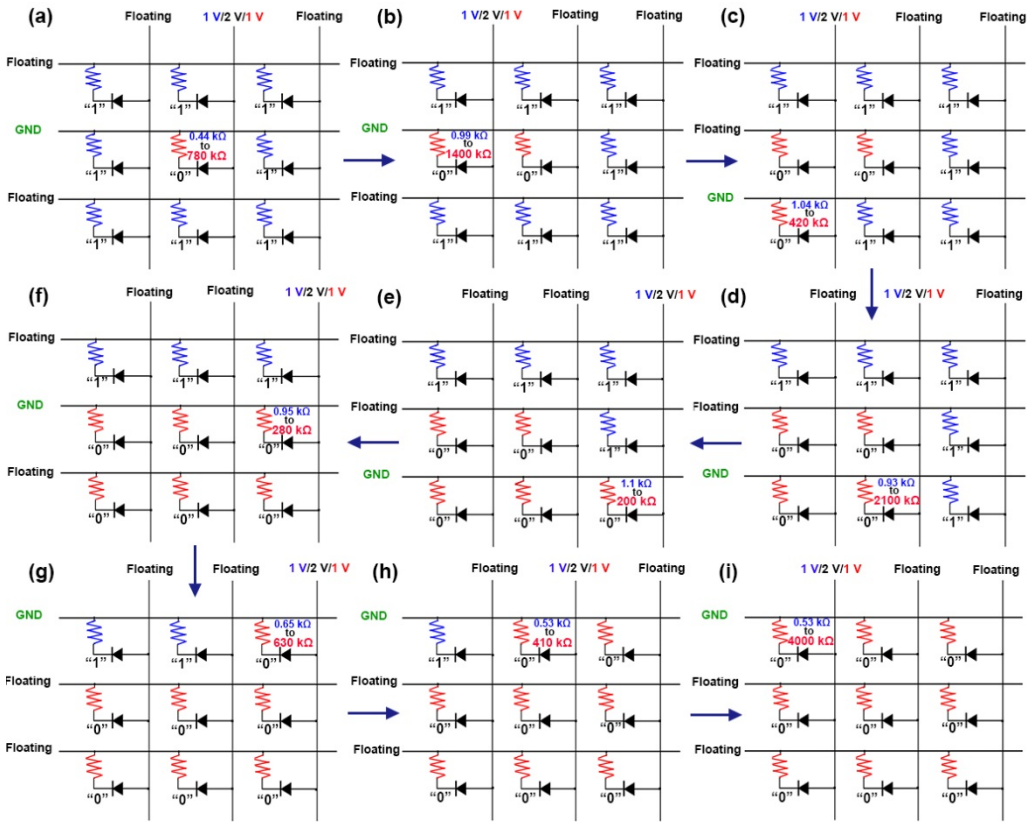


**Fig. S13.** The erasing process of 3 × 3 flexible 1D-1R RRAM cells. Red color denotes the HRS (logic state "0") and blue color denotes the LRS (logic state "1").

REFERENCES


1. J. H. Ahn, H. S. Kim, K. J. Lee, S. Jeon, S. J. Kang, Y. G. Sun, R. G. Nuzzo, J. A. Rogers, *Science* **2006**, *314*, 1754.
2. E. Menard, K. J. Lee, D. Y. Khang, R. G. Nuzzo, J. A. Rogers, *Appl. Phys. Lett.* **2004**, *84*, 5398.
3. H. S. P. Wong, H. Y. Lee, S. M. Yu, Y. S. Chen, Y. Wu, P. S. Chen, B. Lee, F. T. Chen, M. J. Tsai, *Proc. IEEE* **2012**, *100*, 1951.
4. K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, Y. Sugiyama, *Appl. Phys. Lett.* **2008**, *93*, 033506.
5. G. H. Kim, J. H. Lee, Y. Ahn, W. Jeon, S. J. Song, J. Y. Seok, J. H. Yoon, K. J. Yoon, T. J. Park, C. S. Hwang, *Adv. Funct. Mater.* **2013**, *23*, 1440.
6. A. Rose, *Phys. Rev.* **1955**, *97*, 1538.
7. A. Many, S. Z. Weisz, M. Simhony, *Phys. Rev.* **1962**, *126*, 1989.