

# Giga-seal solvent-free bilayer lipid membranes: from single nanopores to nanopore arrays

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## Supplementary Information

### S1 Experimental Section

#### GUV Preparation

Giant unilamellar vesicles (GUVs) were prepared by the electroformation technique.<sup>1, 2</sup> Briefly, 50  $\mu\text{l}$  of 1 mg/ml solution of lipid (pure DPhyPC, or 99:1 (w/w) DPhyPC/NBD-DMPE) in chloroform were spread dropwise over an area of  $\sim 10\text{ cm}^2$  of a glass plate coated with In/Ti oxide (ITO) and dried in vacuum overnight. After drying, two lipid-coated glass plates were clamped against each other with a 1 mm thick PDMS spacer in between. The gap between the glass plates was filled with a 180 mM sucrose solution in water. An electrical contact was made from a signal generator (Pulse-/Function Generator PGS201) to the lipid-coated ITO surfaces. Sinusoidal voltage of 1 V RMS at 10 Hz was applied between the glass plates to induce lipid swelling and GUV formation. After two hours, the suspension of GUVs in sucrose was removed from the cell and transferred to a plastic vial. GUV suspensions were stored at 4°C for up to two weeks. Polydisperse suspensions of GUVs of diameters ranging from a few up to 100  $\mu\text{m}$  were obtained repeatedly using this procedure.

#### GUV/sBLM Imaging by Light Microscopy

GUVs and sBLM (supported lipid bilayer) patches formed by rupture of the vesicles were imaged under the Axioskop upright optical microscope (Carl Zeiss GmbH, Oberkochen, Germany) either in fluorescence or DIC mode. In the fluorescence mode, light emitted by NBD-DMPE from the GUV lamella was filtered via filter set no. 09 (Zeiss) and grabbed by an AxioCam Color CCD camera (Zeiss). The camera signal was read using AxioVision 2.05 software (Zeiss). Image capture in the DIC mode was carried out by means of a uEye UI-1540-C CMOS camera (IDS GmbH, Obersulm, Germany) controlled from the uEye Demo software (IDS).

#### Fabrication of Nanopores by FIB

An SiN TEM window was mounted horizontally on the Nova 600 NanoLab stage with the pit side facing up. The chamber was evacuated and the electron beam was focused and aligned. Subsequently, the pore fabrication site was located on the sample and brought into eucentric height relative to both beams. The stage was tilted perpendicular to the ion beam. The ion beam was focused and aligned in the vicinity of the milling site. The desired configuration of features to be

milled was selected and the material was sputtered off by repeated scanning of the ion beam over the milling pattern. Table S1 gives an overview of typical milling parameters.

**Table S1.** Milling pattern parameters for fabrication of nanopores through 100-nm-thick SiN diaphragms via FIB.

Parameter	Setting
pore count	1-12
nominal pore diameter	50 – 800 nm
pore center-to-center distance	0.25 – 2 $\mu\text{m}$
apparent milling depth	100 – 150 nm
beam dwell time	10 $\mu\text{m}/\text{pixel}$
scan form	circular
scan direction	outer-to-inner
milling sequence	series

#### Coating of SiN TEM Windows for Capacitance Reduction

For single-channel current recordings, the pit side of a SiN TEM window was coated with a thin layer of image-reversal photoresist. A circular region of the photoresist film ( $\sim 50\text{ }\mu\text{m}$  in diameter, centered at the pore-bearing spot) was exposed to UV light and dissolved in developer. The window was further treated with UV-ozone and/or  $\text{O}_2$ -plasma and/or fresh piranha solution to completely remove the photoresist from the pores. The photoresist film was then polymerized at 170°C for 2 hours. This procedure resulted in effective chip capacitances of  $\sim 50\text{ pF}$ .

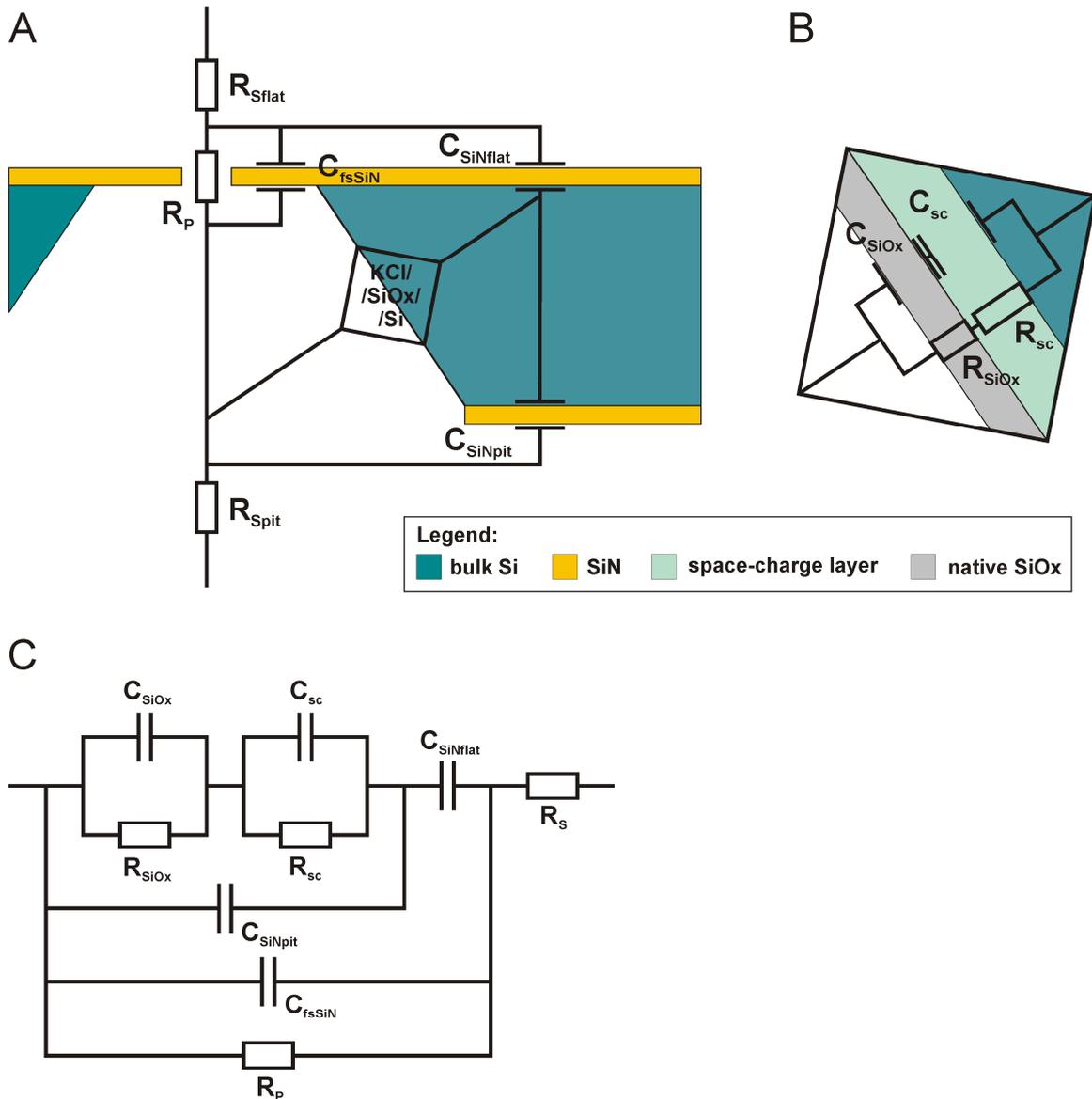
### S2 An Elaborate Electrical Scheme of an SiN TEM Window

Figure S1 shows a schematic of a pore-bearing TEM SiN window based on a *conductive Si frame* that is used as a partition between two electrolyte compartments. The electrical circuit representation of the different subsections of the window, electrolyte and electrodes is superimposed over the schematic.  $R_{\text{SiNflat}}$  and  $R_{\text{Spit}}$  represent the ohmic resistance of the electrolyte and the Ag/AgCl electrode on each side of the window.  $R_{\text{p}}$  is the pore resistance introduced previously.  $C_{\text{fSiN}}$  is the capacitance of the thin free-standing SiN diaphragm. The heterogeneous frame of the window is further subdivided into the following homogeneous subsections and interfaces: the SiN film covering both sides of the frame, represented in capacitive terms by  $C_{\text{SiNflat}}$  and  $C_{\text{SiNpit}}$ , and the pit walls, represented in section A of the figure by the

rhomboid region. The resistance of the silicon bulk is negligible. Section B depicts the scheme of the pit wall sub-circuit, a double RC loop - ( $R_{\text{SiOx}}C_{\text{SiOx}}$ ) and ( $R_{\text{sc}}C_{\text{sc}}$ ) - in full detail. The ‘SiOx’ descriptor refers to 1-2 nm thick layer of native silicon oxide on the walls of the pyramidal pit. The layer forms spontaneously upon exposure of a clean silicon surface to water.  $R_{\text{SiOx}}$  and  $C_{\text{SiOx}}$  represent the resistance and the capacitance of the native oxide film, respectively.  $R_{\text{sc}}$  and  $C_{\text{sc}}$  are the resistance and the capacitance of the space charge layer that develops at the silicon-electrolyte interface. The

equivalent circuit is redrawn clearly in section C.  $R_{\text{Sflat}}$  and  $R_{\text{Spit}}$  are summed up as  $R_{\text{S}}$ .

$R_{\text{SiOx}}$ ,  $R_{\text{sc}}$  and  $C_{\text{sc}}$  are all functions of bias potential of the TEM window silicon frame. As our setup did not provide control of the window potential, the potential was free to float. The impedance properties of the window in the medium range of frequencies hence oftentimes drifted in the course of an experiment. An example of such impedance variance can be seen, for example, in Figure 8b in the frequency range of 1 Hz to 1 kHz.



**Figure S1.** Cross-section schematic of a pore-bearing TEM SiN window. The window is divided into electrically homogeneous subsections. A circuit scheme comprising resistive and capacitive elements that correspond to the respective subsections is overlaid over the schematic. The electrolyte/native-SiOx/Si interface at the pit walls is represented by a rhombus in (A) and illustrated in full detail in (B). (C) Full equivalent electrical circuit corresponding to a pore-bearing SiN TEM window mounted as a partition between two compartments of electrolyte.

## References

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2 S. L. Veatch, in *Lipid Rafts*, ed. T. J. McIntosh, Humana Press, 2007, pp. 59-72.