Supplementary Information for

# Core-Shell $Si_{1-x}Ge_x$ Nanowires with Controlled Structural Defects for Phonon Scattering Enhancement

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**2-point I-V curve data**

**Table S1**. The top, bottom and average diameters of the tapered $Si_{1-x}Ge_x$ alloy nanowires, which are used to calculate the electrical resistivity via 2-point measurement

| Top diameter (nm) | Bottom diameter (nm) | Average diameter (nm) | Channel length (µm) |
|---|---|---|---|
| 77 | 333 | 250 | 4.2 |
| 225 | 381 | 303 | 3.7 |
| 350 | 476 | 413 | 4.4 |
| 473 | 613 | 543 | 3.6 |
| 574 | 668 | 621 | 3 |
| 575 | 825 | 700 | 3.6 |

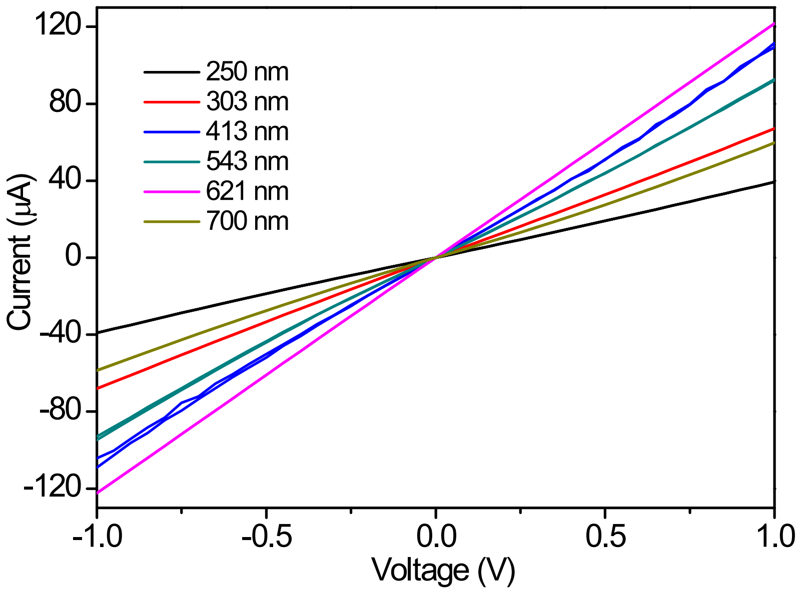


**Figure S1.** I-V curves of tapered $Si_{1-x}Ge_x$ alloy nanowires. The contact between nanowire and metal electrodes shows ohmic behavior.

## 4-point measurement of electrical conductivity

Based on 4-point method, we measured the resistivity of SiGe alloy nanowire (d = ~80 nm) which has similar structure and composition with SiGe alloy nanowire mentioned in manuscript.[S1] We confirmed that the resistivity is ~35 mΩ·cm which is very similar to the values obtained using 2-point measurement. Considering that contact problem becomes serious when diameter of nanowire is small[S2] and tapered nanowires show ohmic behavior, we infer that resistivity error from contact resistance is not significant.

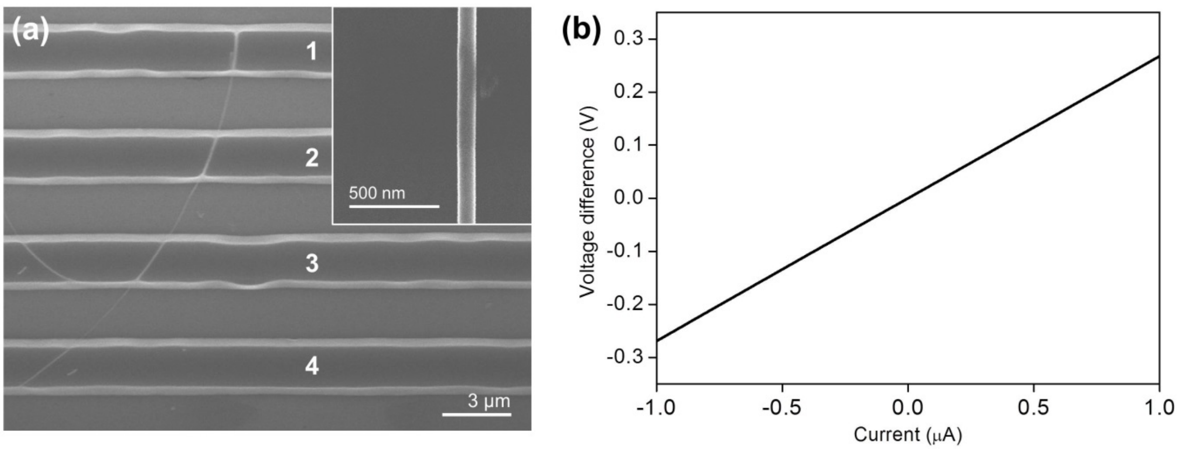


**Figure S2**. (a) A SEM image of the 4-point measurement device. (b) Applied current vs. voltage difference between electrode 2 and 3.

**Thermal properties measurement of tapered $Si_{1-x}Ge_x$ alloy nanowires**

The as-grown nanowires were loaded on micro-fabricated devices by using a solution drop-dry method for measuring the thermal properties.[S3-S5] Before the loading, nanowires were dipped into BHF (5:1) to remove the oxide layer and cleaned by deionized water. This device has two adjacent membranes suspended by silicon nitride beams (inset of Fig 3(b)). Each membrane has a platinum resistance thermometer coil, which serves as a heater and a temperature sensor. Underlying Si substrate was etched by tetramethylammonium hydroxide (TMAH) solution to prevent a heat transfer through the silicon substrate. Thermal contact resistance was reduced by depositing Pt layers by using a focus ion beam (FIB) system at the junctions between nanowires and membranes, and annealing samples at 600 $^{o}C$ in high vacuum (< $10^{-6}$ Torr).

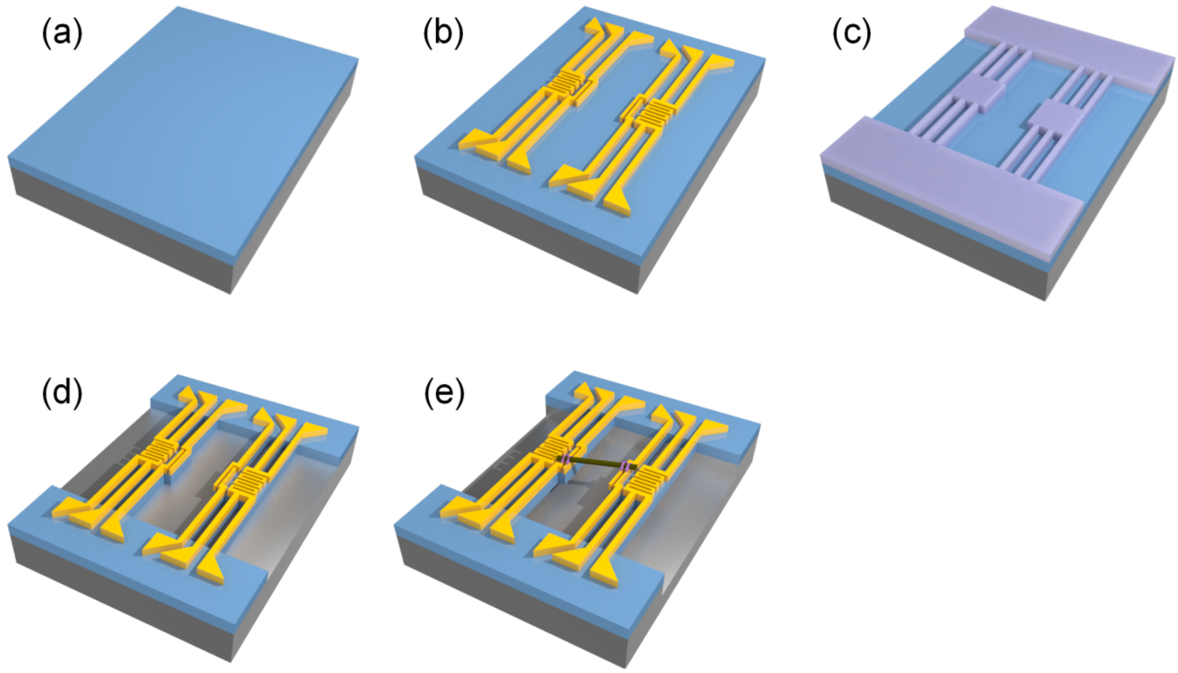


Fig. S3. A schematic of the micro-fabricated MEMS device for measuring nanowire thermal conducvitiy. (a) $SiN_x$ deposition on Si substrate, (b) Patterining the heating and sensing membrane, (c) Photo lithography, (d) $SiN_x$ and Si substrate etching, (e) Pt deposition using a FIB

**Supporting References**


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