Copper-Silicon Core-Shell Nanotube Arrays for Free-Standing Lithium-ion Battery Anodes

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Experiments details

Silicon nanowire template preparation: The vertically aligned silicon nanowire array was prepared using the same technique reported previously [1] with some modification. Briefly speaking, a thin layer of silver was deposited on a silicon wafer by electron beam evaporation and the wafer was then annealed in a quart tube at 600 degree under Argon atmosphere for several minutes to form Ag particles pattern. A Ti/Au bi-layer was sequentially deposited on the Si wafer and the sacrificial Ag particles were removed by ultrasonic to obtain a catalyst mesh. Finally, the wafer was immersed into an etching solution to obtain a vertically aligned SiNW array.

Copper-silicon core-shell nanotube arrays fabrication: After the preparation of silicon nanowire arrays, copper was deposited using a Denton RF/DC magnetron sputtering system. Following copper deposition, the sample was immersed into KOH (1 mol/L) etchant solution at 80^{o}C for several minutes, the copper nanotube array was delaminated from the silicon wafer. At last, amorphous silicon was deposited through a Cello plasma enhanced CVD (PECVD) system.

Structural Characterization: The structure and morphology of the prepared products were characterized by a Raman system (WITec) with a 532 nm wavelength laser, field-emission scanning electron microscopy (SEM, LEO 1550 Gemini) and Transmission electron microscopy (TEM, JEM 2100F JEOL), respectively.

Electrochemical Characterization: Electrochemical characterizations were carried out using CR-2032 coin cell, which was assembled in a high purity Ar filled glove box (H_2O< 0.5 ppm, O_2 < 0.5 ppm, Innovative Technology) with a pure Lithium foil as the counter and reference electrode. The electrolyte used was 1 M lithium hexafluorophosphate ($LiPF_6$) dissolved in ethylene carbonate and dimethyl carbonate (EC/DMC, 1:1 by volume). The galvanostatic discharge-charge measurement and cyclic voltammetry wrere conducted through using a multichannel battery tester (Neware, BTS-610) and an electrochemical workstation (AUTOLAB, M 101), respectively.

Supplementary Figure

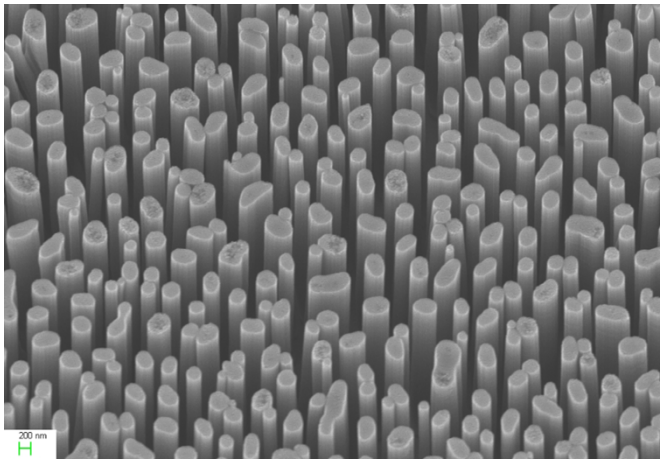

Figure. S1 Tilted SEM image of silicon nanowire arrays template.

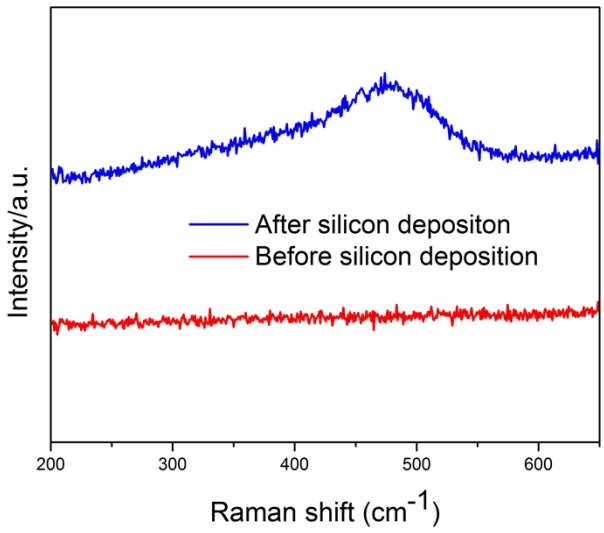

Figure. S2 Raman spectrum of the copper nanowtube arrays before and after amorphoous Si coating. Before coating, there was no raman peaks for copper within this range [2], After amorphous silicon coating, a broad peak at ~480 cm^{-1} can be detected, indicating the characteristic band of amorphous Si [3].

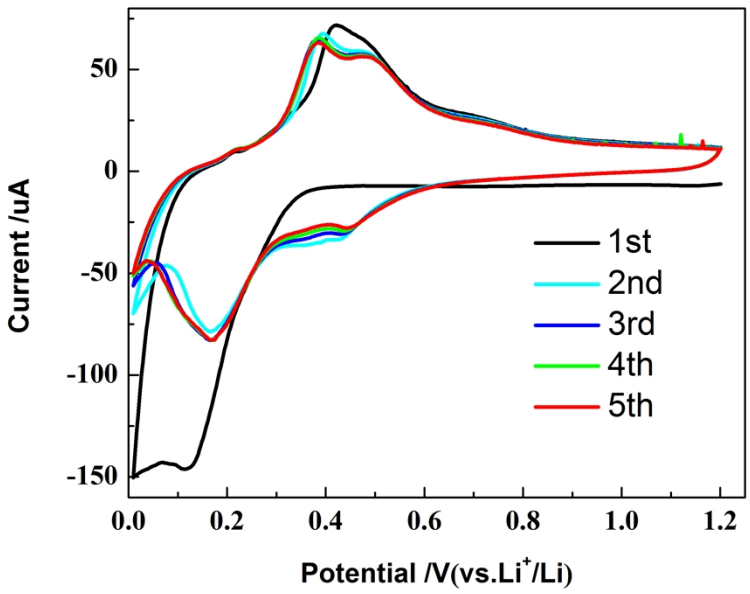

Figure. S3 CV curves of the copper-silicon anode for the first 5 cycles which are corresponding to the results of other amorphous silicon based electrodes [4].

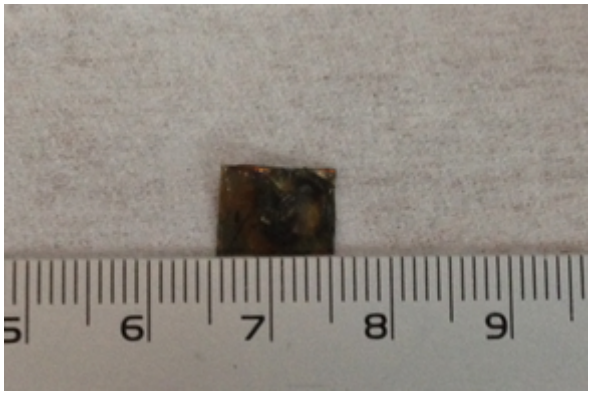

Figure. S4 Photograph of copper nanotube array current collector.

Reference

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3 K. Evanoff, J. Benson, M. Schauer, I. Kovalenko, D. Lashmore, W. Jud Ready and G. Yushin, ACS Nano, 2012, 6, 9837-9845.

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