

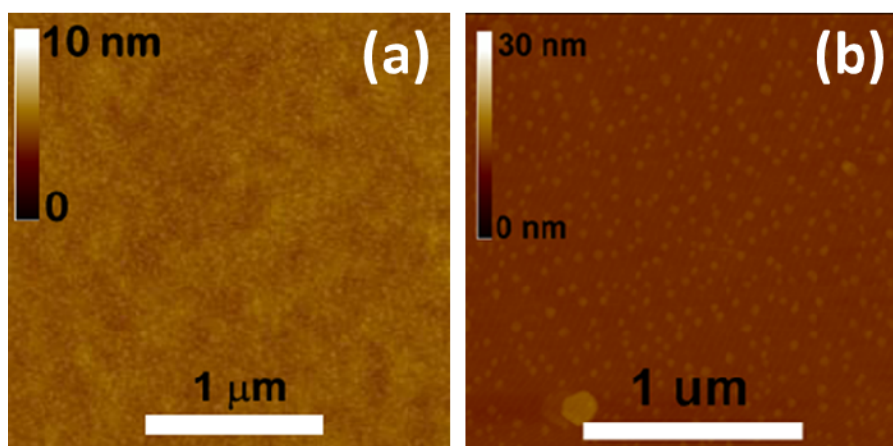
## Electronic Supplementary Information (ESI)

### Low-voltage Flexible Pentacene Thin Film Transistors with Solution-processed Dielectric and Modified Copper Source-drain electrodes

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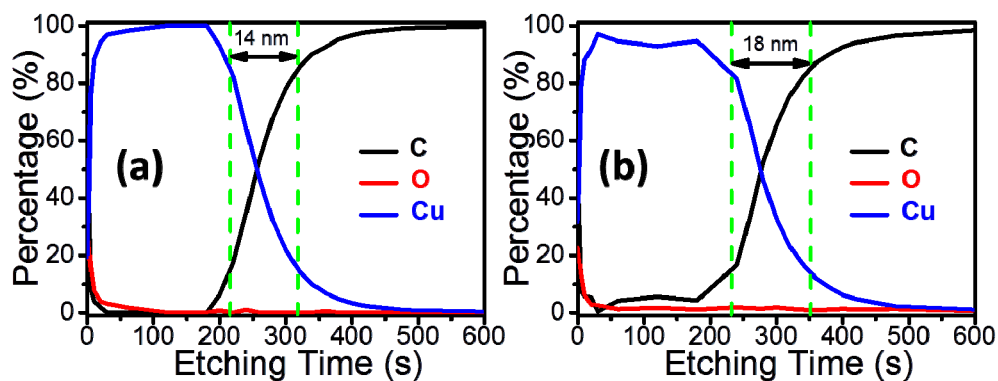
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**Fig. S1** AFM images of solution-processed ATO (a) and ODPA/ATO (b).

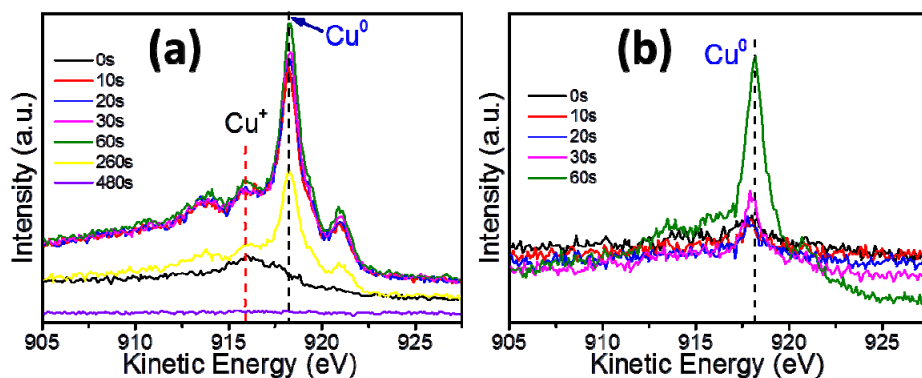
Fig. S1a shows the AFM image of ATO. The root mean square (RMS) roughness value of the solution-processed high-*k* ATO is about 0.2 nm. Fig. S1b shows the AFM image of ODPA/ATO.

Some small clusters can be found on the surface of ODPA/ATO, which is assigned to the residual ODPA molecules. The obtained RMS roughness is about 0.4 nm.



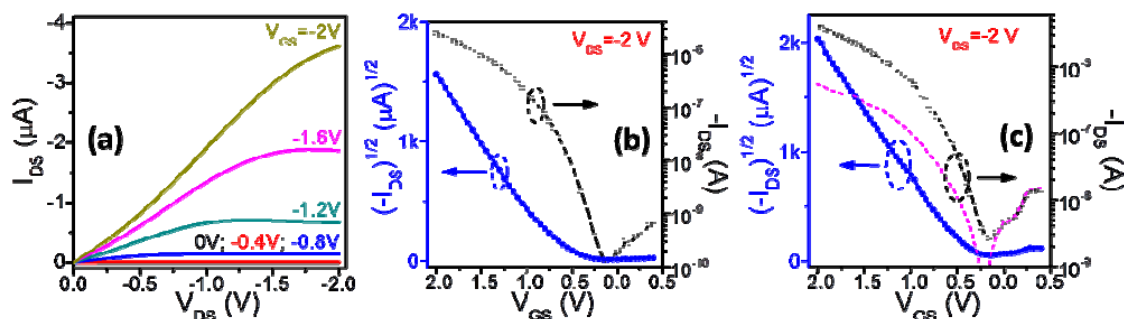
**Fig. S2.** SPX depth profile of (a) *M*-Cu and (b) Cu electrodes on pentacene.

Fig. S2 shows the comparison of XPS depth profile of different electrodes on pentacene. As can be seen from figure S2 that, an obviously sharper interface is observed in the case of *M*-Cu than that in the case of Cu, which deposited at higher vacuum condition ( $3 \times 10^{-4}$  Pa). For clarity, we define the region with carbon (C) signal varying from 15% to 85% as the interface region between electrode and pure pentacene layer. The interface layer thickness of *M*-Cu is about 14 nm, while that of Cu is about 18 nm. The sharp interface in the case of *M*-Cu might be due to the fact that, the in-situ oxidized Cu in the initial stage of thermal evaporation can act as a shield which preventing the diffusion of the Cu atoms into the underneath pentacene layer.



**Fig. S3.** Cu *LMM* Auger spectra of (a) 40 nm *M*-Cu and (b) 10 nm Au encapsulated 30 nm *M*-Cu (Au/*M*-Cu) S/D electrodes on pentacene as a function of etching time.

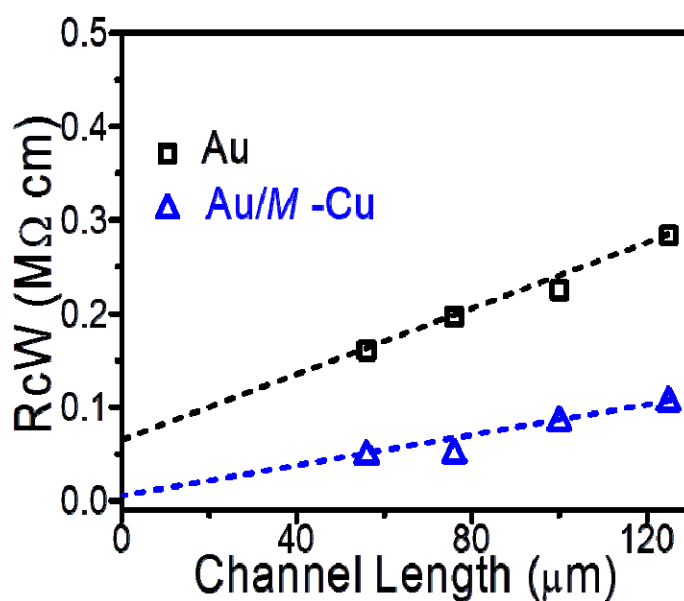
Fig. S3 shows the variation of Cu *LMM* Auger spectra of different electrodes with etching time. As can be seen from Fig. S3a, the top surface of the *M*-Cu film exhibits only one peak at ~916 eV, which can be assigned to Cu<sup>+</sup>, indicating the completely oxidation of Cu. With increasing the etching time, another peak located at ~918 eV begins to appear, which corresponds to the metallic Cu<sup>0</sup>. In addition, with prolonging the etching time, the peak intensity of ~918 eV increases, while that of ~916 eV decreases and disappears after 60 s, implies the gradual transition from oxidized state to metallic state of *M*-Cu electrodes. On the other hand, at 260 s, which corresponding in the interface region between electrodes and pentacene layer, this peak emerges again, confirming the oxidation of Cu at the initial stage of thermal deposition. When encapsulated with 10 nm Au, the only peak observed in the Cu *LMM* Auger peak at ~918 eV is ascribed to the Cu<sup>0</sup>, manifesting that the oxidation of Cu is effectively prevented by Au encapsulation, as shown in Fig. S3b.



**Fig. S4.** (a) Output and (b) transfer curves of flexible pentacene TFT with 40 nm Au S/D electrodes, (c) transfer curves of flexible device with AT0 as gate dielectric and Au/M-Cu as S/D electrodes, the dashline gives the gate leakage current.

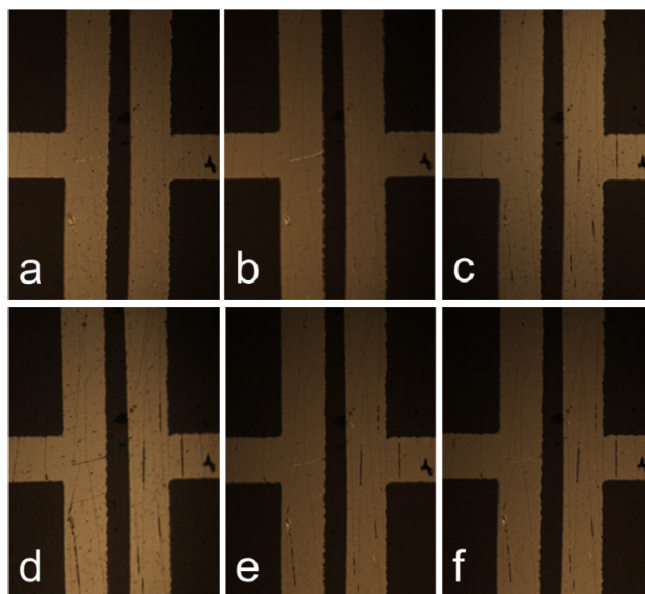
Fig. S4a shows the output curves of the device with 40 nm Au S/D electrodes. Due to the high quality of the ODPA/ATO system, no obvious leakage is detected near zero  $V_{DS}$ . The saturation current is about  $3.6 \times 10^{-6}$  A at  $V_{DS} = V_{GS} = -2$  V. However, the curves exhibit apparent “S” shape at low  $V_{DS}$ , which is an indication of contact effect, resulting from the high contact resistance. Fig. S4b gives the corresponding transfer curves. The extracted on/off ratio,  $\mu$ ,  $V_T$  and  $SS$  are estimated to be  $10^4$ ,  $0.6 \text{ cm}^2/\text{Vs}$ ,  $-0.7$  V and  $182 \text{ mV/dec}$ , respectively. Fig. S4c exhibits the transfer curves of the flexible device with AT0 as gate dielectric and Au/M-Cu as S/D electrodes. The device possesses much lower electronic properties than that with ODPA/ATO as gate

dielectric, with on/off ratio and  $\mu$  values of  $10^3$  and  $0.6 \text{ cm}^2/\text{Vs}$ , respectively. The low performance can be ascribed to the high leakage and large surface energy of the ATO.



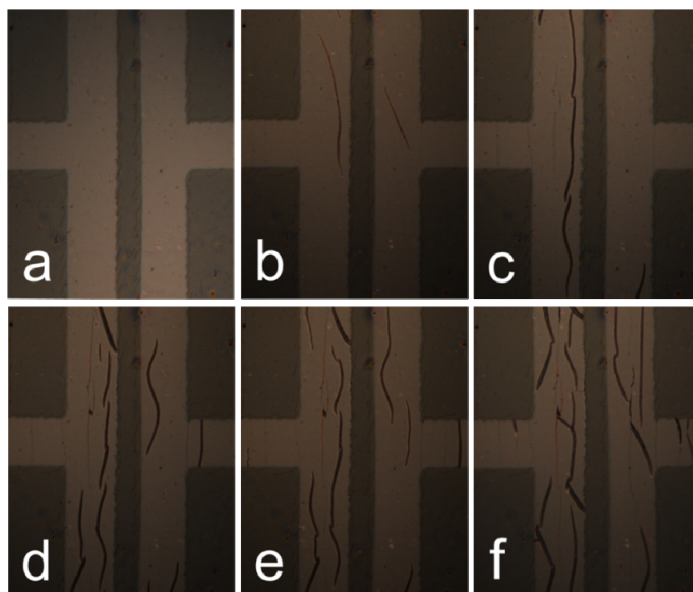
**Fig. S5.** Channel-width-normalized contact resistance ( $R_{cW}$ ) as a function of channel length of devices with Au and Au/M-Cu electrodes.

Fig. S5 plots the  $R_{cW}$  as a function of channel length of devices with Au and Au/M-Cu electrodes. The  $R_{cW}$  obtained by transfer line method (TLM) are  $6.2 \times 10^{-2} \text{ MW}\cdot\text{cm}$  and  $3 \times 10^{-3} \text{ MW}\cdot\text{cm}$  for Au and Au/M-Cu electrodes, respectively.



**Fig. S6.** A series of microscopic images of the S/D electrodes during the cyclic bending test under compressive stress: (a) before bending, (b) 10, (c) 100, (d) 500, (e) 1000 and (f) 2000 cycles.

Fig. S6 shows the microscopic images of the S/D electrodes during the compressive bending cycling test. From these images, we can clearly see that the cracking density increases monotonously with bending cycles before 500 times, and keeps almost unchanged up to 2000 bending times.



**Fig. S7.** A series of microscopic images of the S/D electrodes during the cyclic bending test under compressive stress: (a) before bending, (b) 10, (c) 100, (d) 500, (e) 1000 and (f) 2000 cycles.

Fig. S7 shows the variation of electrodes with bending cycles. As seen, the density of cracks increases with bending times. At the same time, the gap in the crack area also increases with bending cycles, which can be due to the delamination of the electrodes from pentacene layer along the crack.