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Electronic Supplementary Information for

Versatile ultra-thin Au nanomesh from reusable anodic aluminium oxide (AAO) membrane

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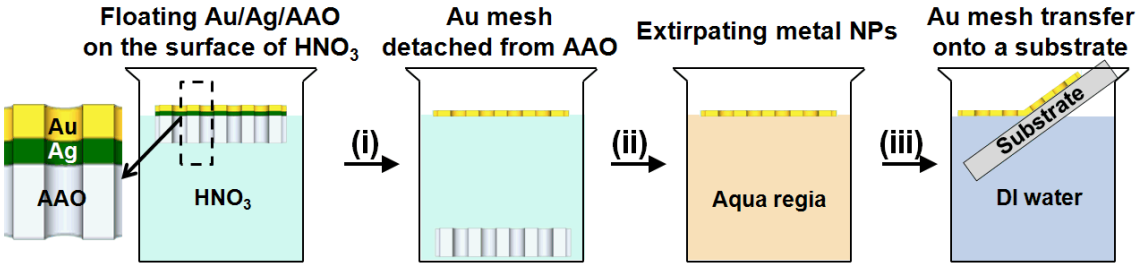
Supplementary Information 1

In this work, Au nanomesh was fabricated by dint of sacrificial wet-etching of Ag layer of Au/Ag/AAO. **Scheme S1** describes the detail for preparation of Au nanomesh. Au/Ag-coated AAO membrane was floated on the surface of HNO_3 solution (60%) to selectively etch away Ag layer from Au/Ag/AAO membrane. Within 10 min, Au layer separated from AAO replication master was floating on the surface of HNO_3 solution. Afterward, weakly bound metal nanoparticles (NPs) at the edges of holes of Au nanomesh were removed by floating the resulting Au mesh on the surface of diluted aqua regia. Finally, Au mesh was transferred onto a substrate after replacing aqua regia with de-ionized (DI) water in order to rinse Au mesh.



Scheme S1 Schematic diagram for transfer of Au mesh on a substrate by (i) selectively dissolving Ag sacrificial layer of Au/Ag-coated AAO by HNO_3 and (ii) extirpating undesired metal nanoparticles (NPs) from the bottom side of the mesh after replacing HNO_3 with aqua regia, followed by (iii) transfer of Au nanomesh after DI water rinsing.

Supplementary Information 2

We measured current-voltage (*I*-*V*) curves of Au nanomesh and thin films prepared on polyethylene terephthalate (PET) substrate. **Fig. S1** shows the measurement configuration used in this work. Au-coated tungsten probe tip was utilized in this work. As shown in **Fig. S1**, in order to measure *I*-*V* curve while bending the sample, the sample was loaded in a plastic box. Two electrical contacts were formed within conducting area (that is, Au mesh and film) at a distance of 3 cm.

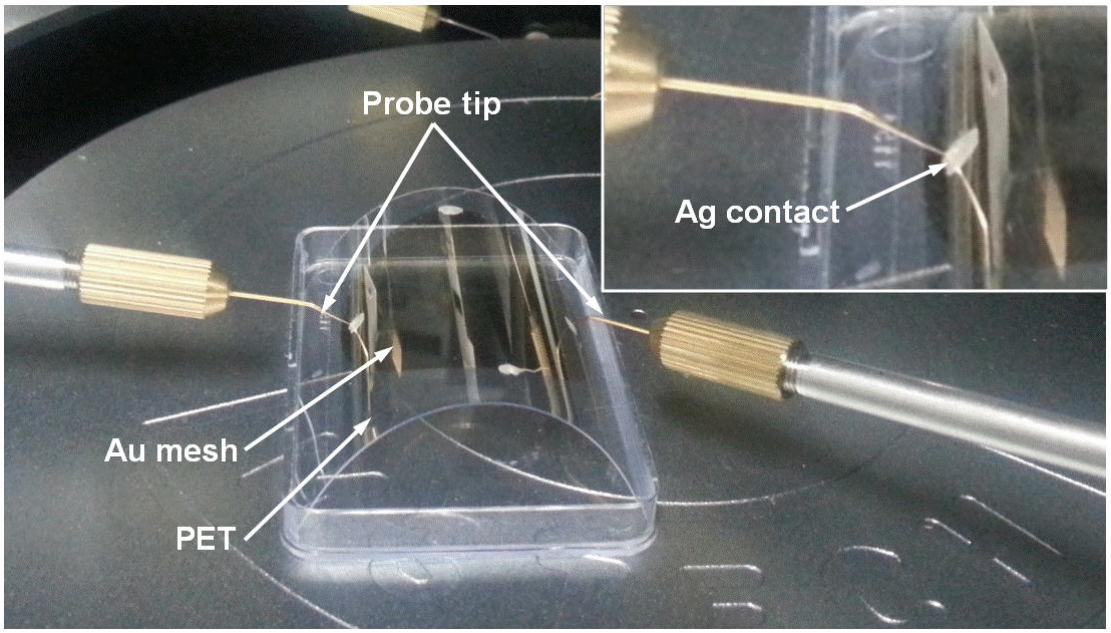


Fig. S1 A photograph of electrical measurement configuration utilized in this study. Inset is a magnified image in the vicinity of the Ag electrical contact.

Supplementary Information 3

In order to ensure complete removal of the Ag layer from Au/Ag-bilayed metal mesh, EDS analysis was performed on the Au nanomesh loaded onto the Si substrate. **Fig. S2** shows the EDS mapping results on the Au nanomesh.

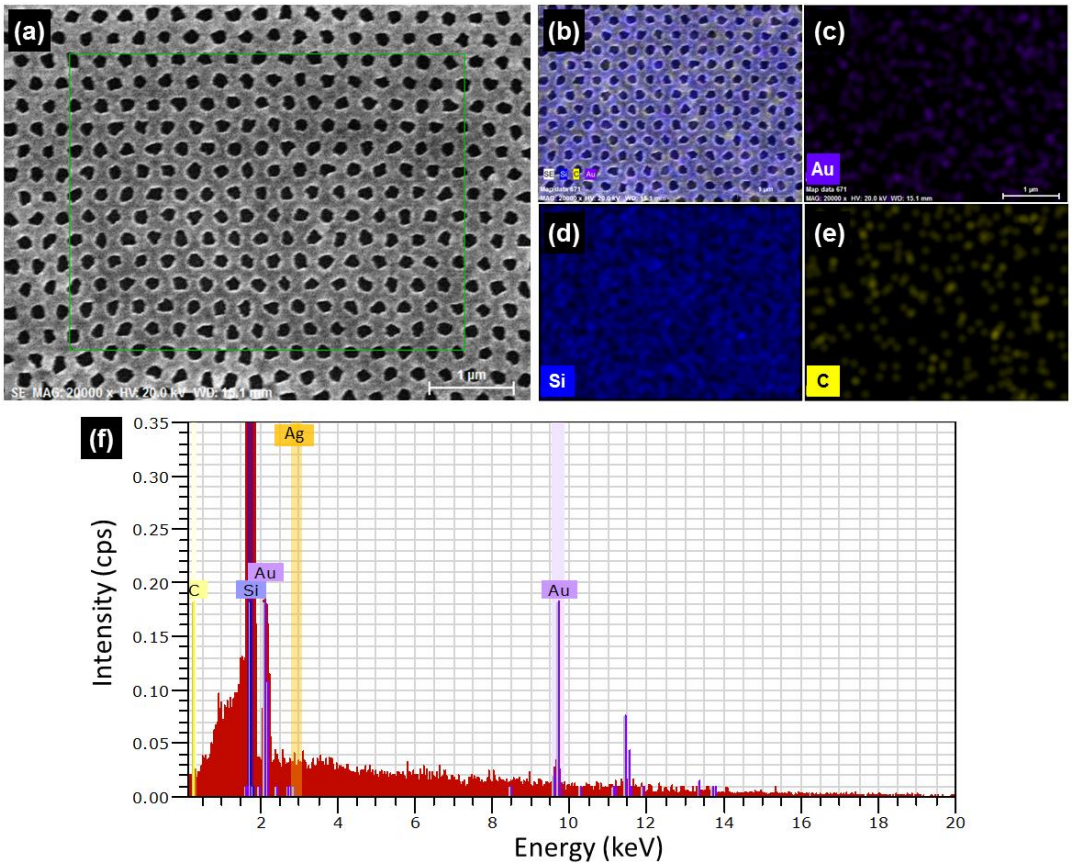


Fig. S2 (a) SEM image of the Au nanomesh and (b – f) EDS elemental mapping results of it on the area enclosed by green square: (b) SEM images with EDS mapping results and elemental mapping results of (b) Au (purple), (d) Si (blue), and (e) C (yellow), and (f) corresponding EDS spectrum with energy range for Ag.

Supplementary Information 4

For the purpose of gain quantitative information on the variation of the porous AAO during etching in HNO_3 (60%), we performed a SEM investigation on the bottom side of the through –hole AAO, which was etched at a different etching time from 0 to 70 min at intervals of 10 min: through-hole AAO was obtained from 24-h anodisation, followed by residual Al etching using an aqueous solution of 3.4 g $CuCl_2 \cdot 2H_2O$, 50-mL of 38 wt% HCl, and 100mL DI water and succeeding pore opening and widening for 100 min by utilizing 5 wt% H_3PO_4 maintained at 29 °C. **Fig. S3** displays the resulting SEM images.

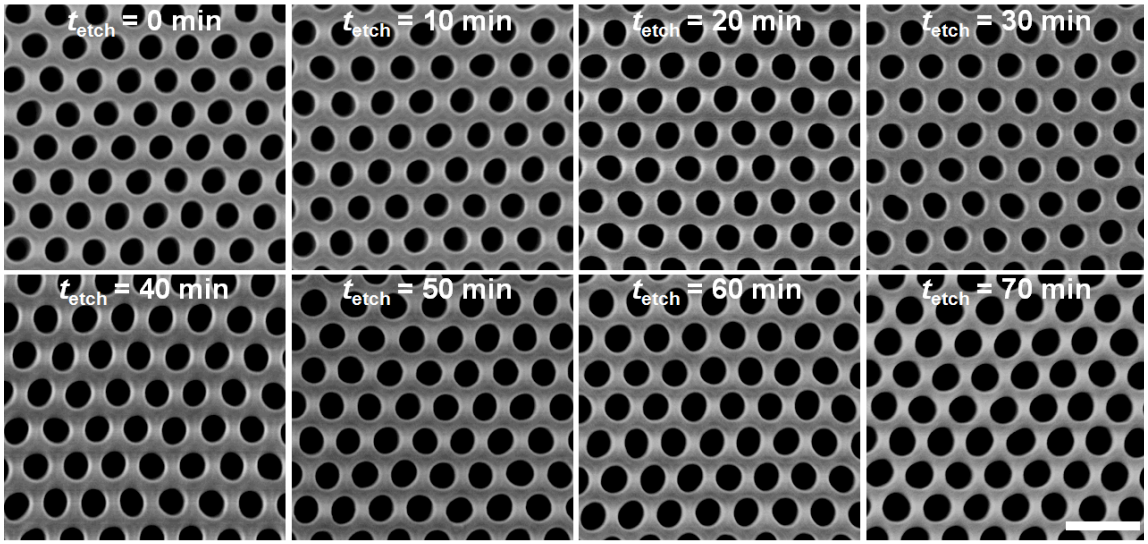


Fig. S3 Representative SEM micrographs of the bottom side of AAO which is etched in HNO_3 (60%) for varied etching time (t_{etch}) from 0 to 70 min at 10-min intervals. Scale bar is 200 nm.

Supplementary Information 5

Fig. S4 shows results of SEM and TEM investigation on the SiNWs obtained from metal-assisted chemical etching (MaCE) of Si(001) substrate. Au nanomesh was replicated from AAO obtained by anodizing Al under 25 V using 0.3 M H_2SO_4. **Fig S4(a,b)** demonstrate control of nanowire length by changing etching time. SiNWs prepared under the present etching conditions using mixture solution of HF and H_2O_2 [HF:H_2O_2 = 2:1 in v/v] are single crystalline with sub-nm surface roughness.

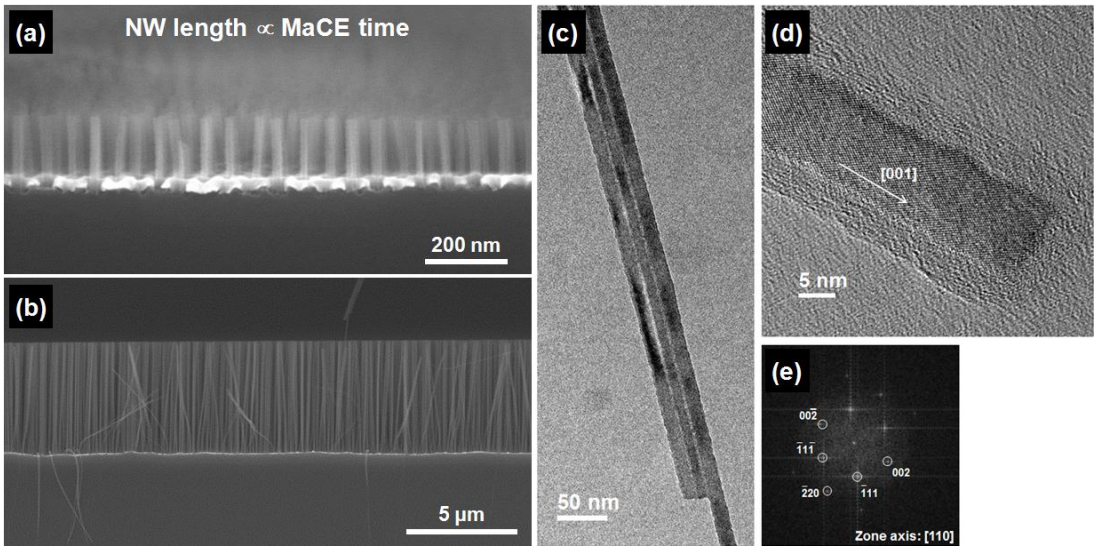


Fig. S4 (a, b) SEM images and (c, d) TEM images of the single crystalline SiNWs fabricated from MaCE of Si(001) substrate by adopting Au nanomesh as an etching catalyst. The corresponding fast Fourier Transform (FFT) pattern is displayed in panel (e).