Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C

Electronic Supplementary Information

Manipulating ZnO Nanowires for Field-effect Device Integration by Optical-fiber Grip Coated with Thermoplastic Copolymer

Pyo Jin Jeon,[‡a] Sejin Lee,[‡b] Young Tack Lee,[a] Hee Sung Lee,[a] Kyunghwan Oh[*b] and Seongil Im[*a]

a Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea. Fax: 82-2-392-1592; Tel:82-2-2123-2842; E-mail: semicon@yonsei.ac.kr

b Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea. Fax: 82-2-392-1592; Tel:82-2-2123-5608; E-mail: koh@yonsei.ac.kr.

*Corresponding authors : (Seongil Im) semicon@yonsei.ac.kr & (Kyunghwan Oh) koh@yonsei.ac.kr

‡ Pyo Jin Jeon and Sejin Lee equally contributed to this work.

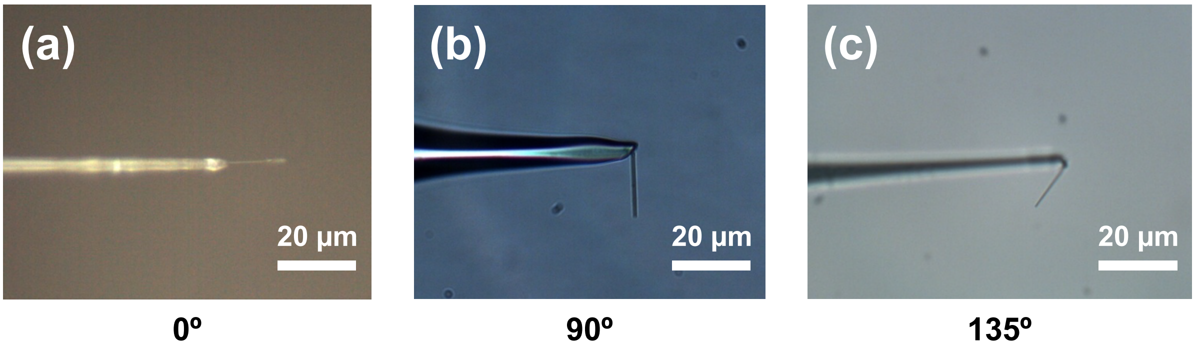

Fig. S1 (a) ~ (c) shows ZnO NWs attached to tapered optical fiber tip with different angles.

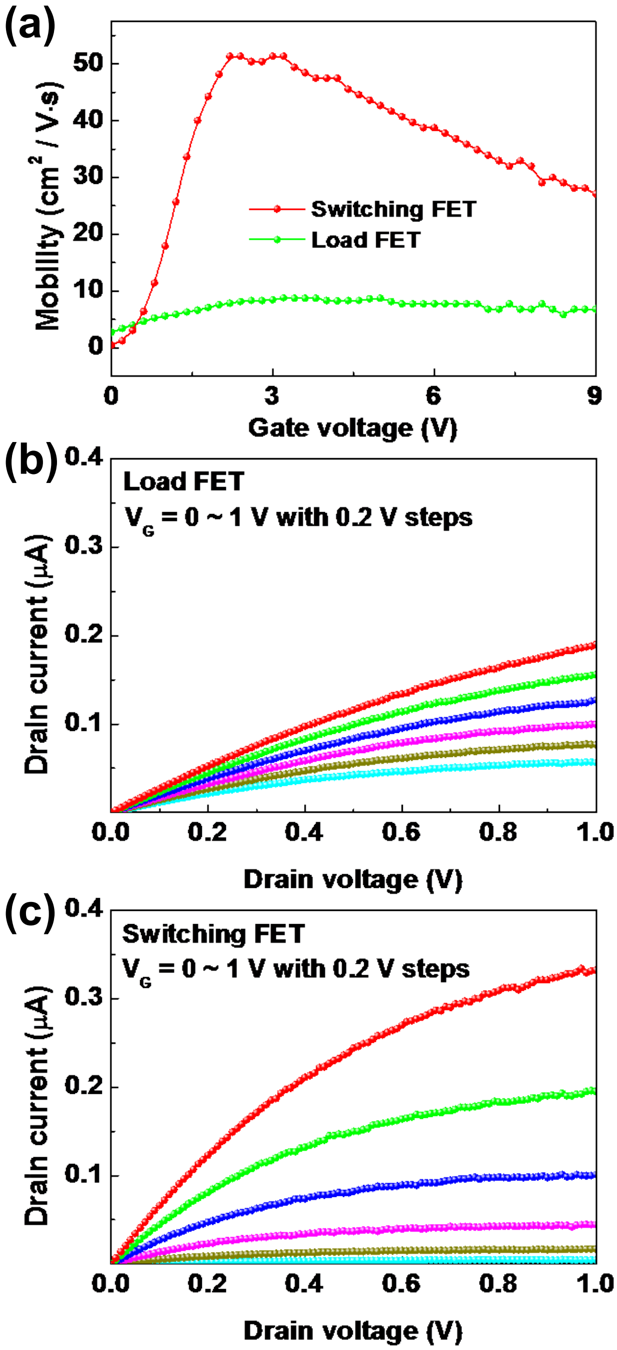

Fig. S2 (a) Linear mobilities as a function of V_G obtained from ZnO NW FETs with the two different NWs that annealed at 400 and 600 ℃ for 30 min in air, respectively for load and switching driver. (b,c) Output curves of the load and switching FETs for depletion-load inverter in a range of V_G = 0~1 V with 0.2 V steps. In order to calculate the mobilities, we used cylindrical core-shell model based on the following equations,

$$\mu = \frac{g_m \times L^2}{C \times V_D} \tag{1}$$

, where transconductance (g_m) and capacitance (C) are given by Eq. (2) and Eq. (3), respectively.

$$g_m = \frac{dI_D}{dV_G}, \qquad (2)$$

$$C = \frac{2\pi\varepsilon_0\varepsilon_{Al_2O_3}L}{\ln[(r+t)/r]} \qquad (3)$$

, where L (5 μm) is the channel length of the FETs, t (30 nm) is the thickness of the gate insulator layer, r (60 and 75 nm) is the wire radius, and $\varepsilon_{Al_2O_3}$ (~7.8) is the dielectric constant of the insulator.

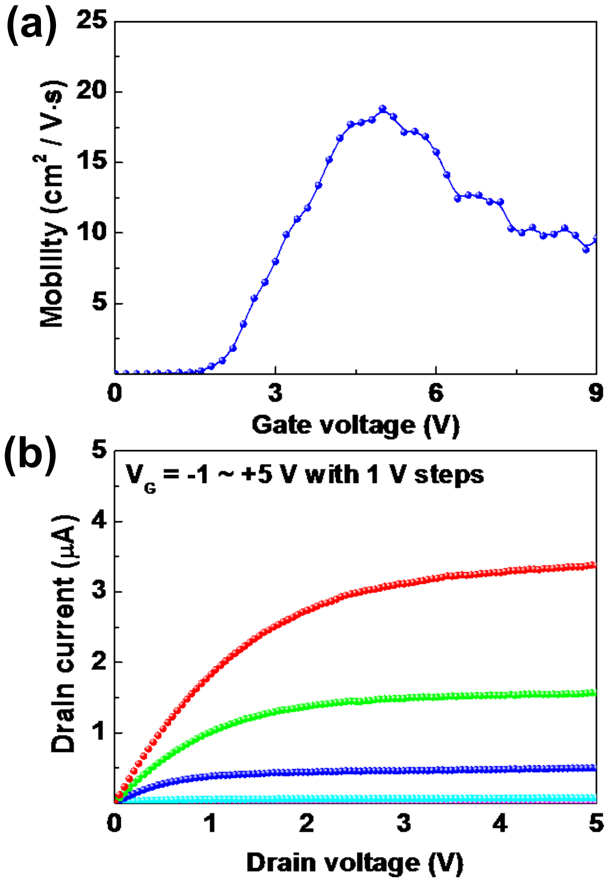

Fig. S3 (a) Linear mobility plot of switching NW FET for our resistive load inverter and (b) its output curves in a range of V_G = 0~1 V with 0.2 V steps.

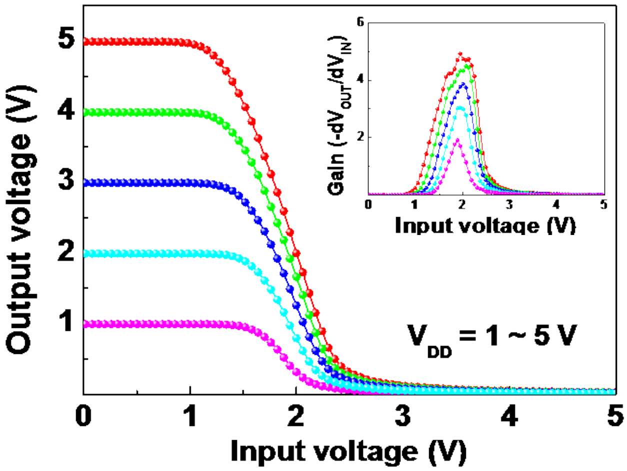

Fig. S4 Voltage transfer characteristics of our resistive load inverter, in a range of V_D = 1~5 V. Inset indicates the inverter voltage gain ($-dV_{OUT}/dV_{IN}$). Higher V_{DD} leads to higher gain.