Electronic Supplementary Material (ESI) for Journal of Materials Chemistry C

Supporting Information

Interface engineering for suppression of flat-band voltage shift in the solution-processed ZnO / polymer dielectric thin film transistor

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Table S1. Definition of the variables used in the analytic model.

Variables	Definition	Values	Units
W	Width of the channel	1000	μm
L	Length of the channel	50	μm
V_G	Gate bias voltage	-	
V_D	Voltage at the drain electrode	30	V
V_S	Voltage at the source electrode	0	V
C_i	Capacitance of the gate-insulator per unit area	9.00	nF cm^{-2}
ε_s	Relative electrical permittivity in ZnO	7.5	-
n_0	Charge-carrier number of ZnO per unit volume	10^{19}	cm^{-3}
T	Temperature of the device	298	K
V_{FB}	Flat-band voltage	Fitting parameter	V
T_0	Trap characteristic temperature	Fitting parameter	K
N_t	Total number of trap state per unit volume at T	Fitting parameter	cm^{-3}
σ_0	Conductivity of ZnO at infinite temperature	Fitting parameter	S cm^{-1}

Table S2. Values of fitting parameters used for the simulation in **Figure 5**.

	ZnO/SAIL/PVP TFT		ZnO/PVP TFT		Units
	Forward	Backward	Forward	Backward	
V_{FB}	0.009	0.499	-2.742	6.014	V
T_0	553	553	550	552	K
N_t	$2.95*10^{19}$	$2.94*10^{19}$	$2.53*10^{19}$	$2.10*10^{19}$	cm^{-3}
σ_0	2.23	2.35	2.25	2.99	S cm^{-1}

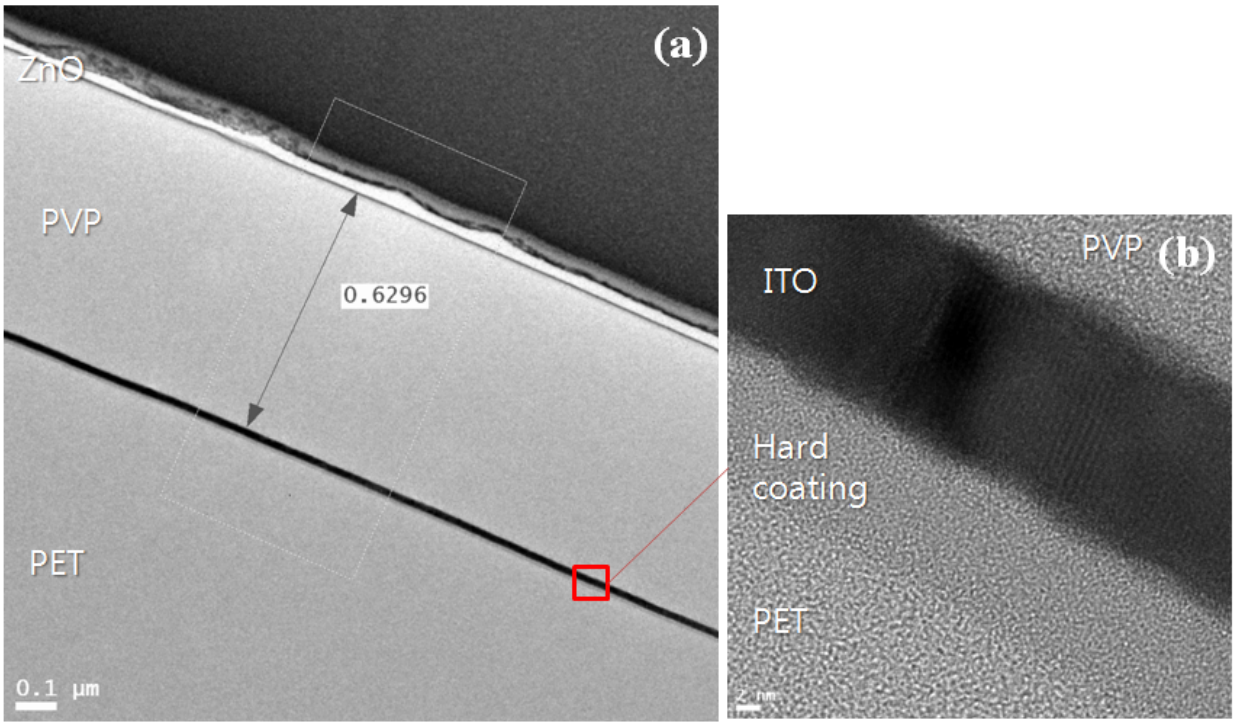

Figure S1. HR-TEM images of solution processed ZnO semiconductor on polymer dielectric layer were shown. (a) The poly crystalline ZnO semiconductor was well deposited on the highly cross linked PVP, c-PVP, dielectric layer with 629 nm thickness. (b) The flexible gate & substrate was fabricated with 20 nm ITO on the polyester (PET) film.

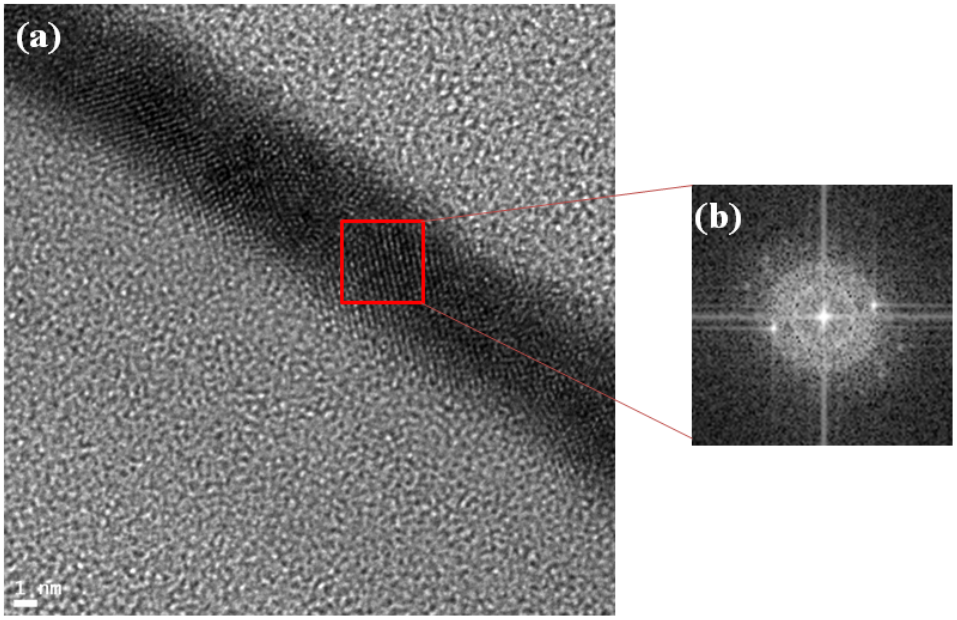

Figure S2. (a) Cross-sectional HR-TEM image of solution processed ZnO semiconductor on polymer dielectric layer were shown. (b) The solution processed ZnO shows crystalline FFT-SAED patterns.

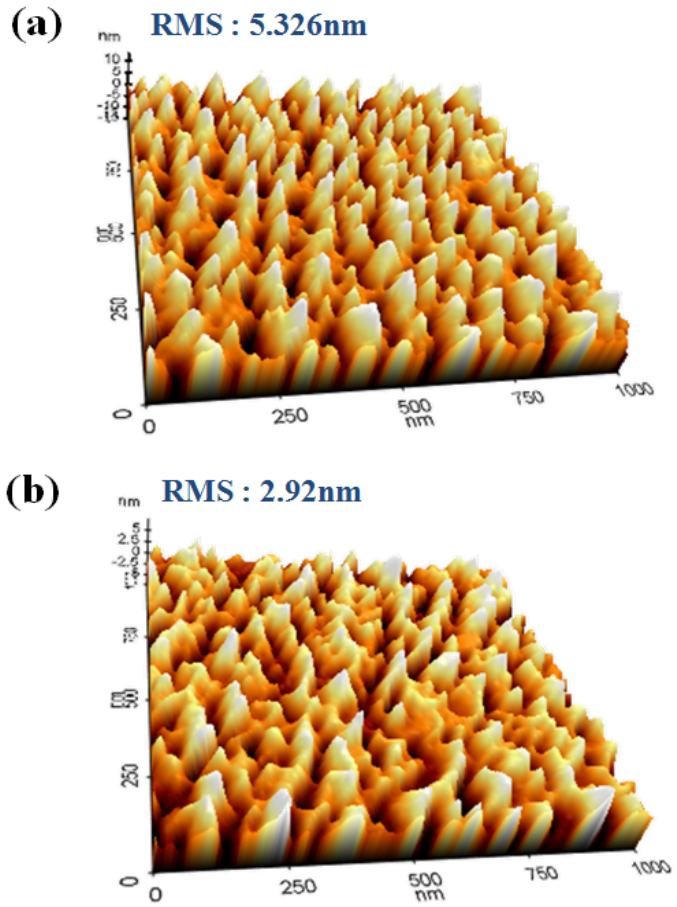

Figure S3. 3D views of AFM images: (a) 3D view of ZnO thin film on PVP without interface engineering (RMS=5.33 nm), (b) 3D view of intrinsic ZnO thin film on PVP with interface engineering (RMS= 2.92 nm)

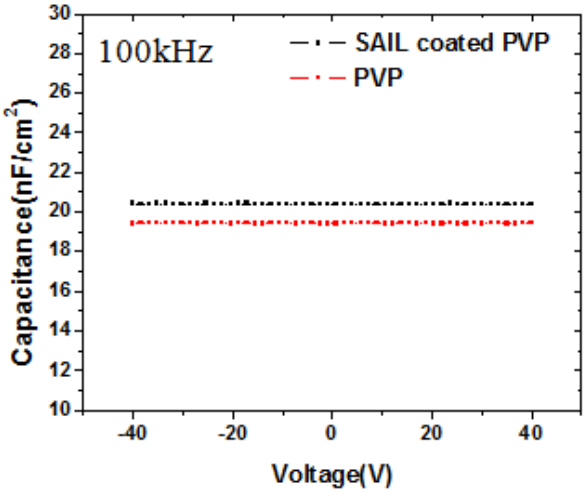

Figure S4. Voltage-dependent capacitance of both the SAIL coated PVP and the intrinsic PVP at 100 kHz.

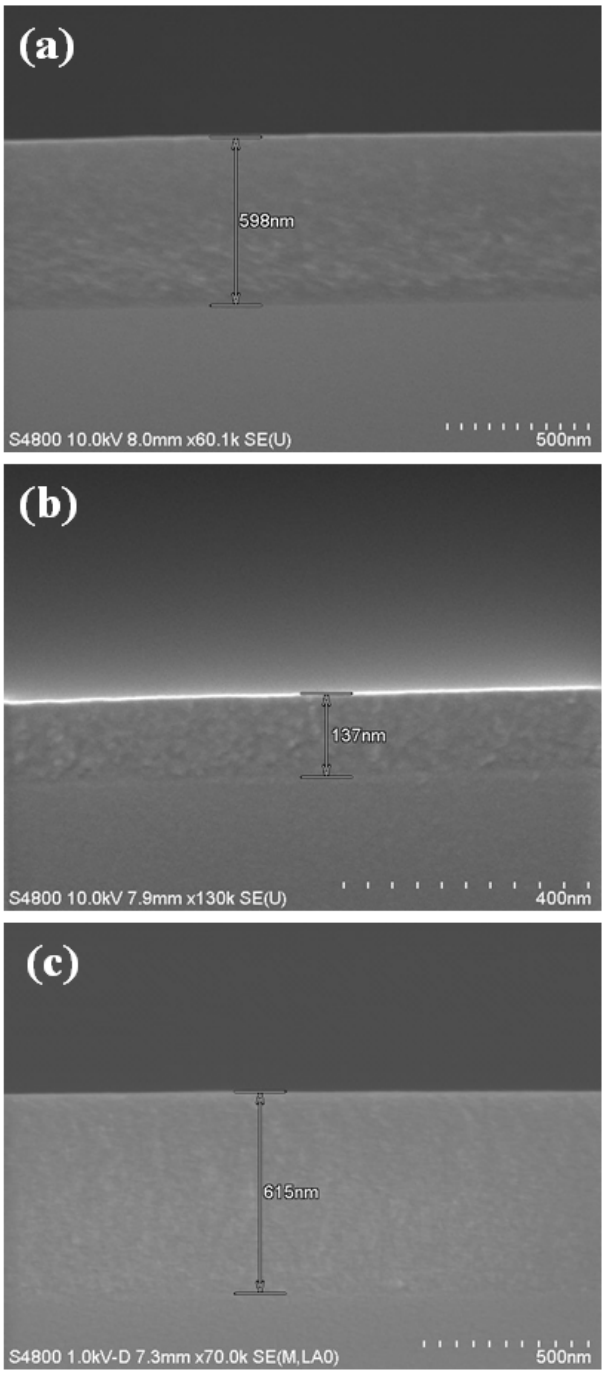

Figure S5. Cross-sectional SEM images of polymer dielectric layers were shown. (a) The thickness of spin-coated PVP at 2000 rpm was 598 nm. (b) The thickness spin-coated TPC at 2000 rpm was 137 nm. (c) The thickness of spin-coated double dielectric layer was 615 nm that is the sum of TPC and PVP layer by spin-coating at 2000 rpm.

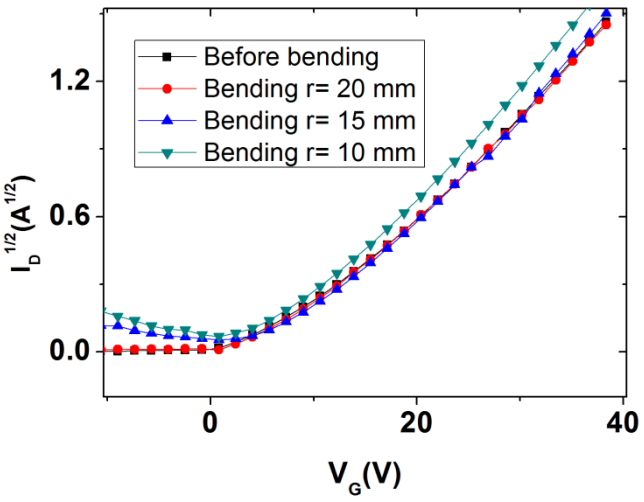

Figure S6. The $I_{DS}^{1/2} - V_G$ transfer curves of the flexible ZnO/SAIL/PVP TFT in accordance with before and during bending.

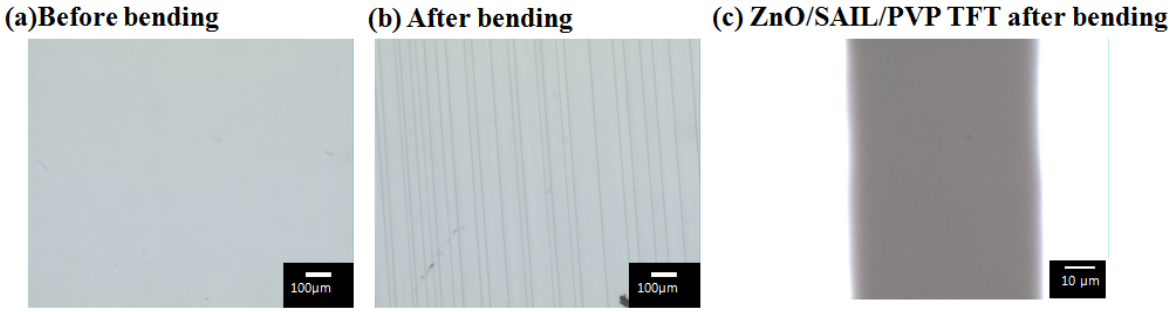

Figure S7. Optical spectroscopy images: (a) the ITO PET before bending; (b) the ITO PET after bending. (C) The ZnO/SAIL/PVP TFT was shown reliable flexibility without any delamination after bending.