

## Supporting information.

# Direct on Chip Cadmium Sulfide Thin Film Transistors Synthesized Via Modified Chemical Surface Deposition

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### Thermal annealing in nitrogen atmosphere

As mentioned in the body of the paper, after the reaction, the films were also annealed at 300°C for 60 min in nitrogen ( $N_2$ ). This is a direct comparison between films not annealed and annealed in air. The resistivity calculated by the transmission line method (TLM) for films annealed in  $N_2$  was in the order of  $\sim 9 \times 10^7 \Omega \cdot \text{cm}$ . Figure 1-Sa, shows the XRD diffraction results for  $N_2$  annealed film. This film exhibited broad peaks at 24.7°, 26.4°, 28.17°, 43.55°, 47.8° and 51.77°, corresponding to the (100), (002), (101), (110), (103) and (112) planes for hexagonal phase of CdS, respectively (JCPDS No. 6-314). The calculated crystallite size was 14.2 nm.

No significant changes were observed in the film morphology after the annealing process in  $N_2$ , as is shown in the SEM results shown in Figure 1-Sb. These results indicate that the annealing atmosphere plays an important role in the CdS films. Dimitrov, *et.al.*,<sup>1</sup> reported that the CdS is more thermally stable under nitrogen than in air, and our results indicate that cyanamide is more stable or just decomposes at slower rate in nitrogen than in air due to the presence of oxygen, in agreement with the literature.<sup>2</sup> This indicates that air annealing is preferred.

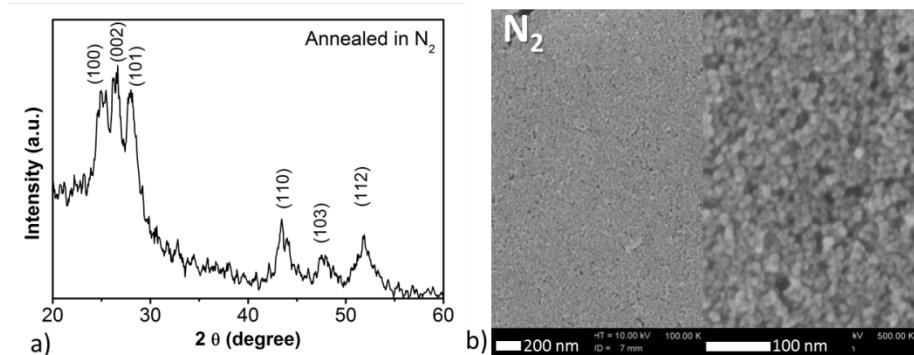


Figure 1-S. a) XRD diffraction pattern for CdS films annealed at 300°C for 60 min in  $N_2$ . b) SEM images for the same films.

### Annealing temperature in air.

In this and previous reports it has been demonstrated that the physicochemical and electrical characteristics of CdS films are not only temperature dependent, but also ambient dependent.<sup>3,4</sup> As reported, the thermal annealing in air results in a resistivity reduction and the annealing temperature was also studied. The CdS films were annealed in air during 60 minutes at temperatures ranging from 150 to 300°C.

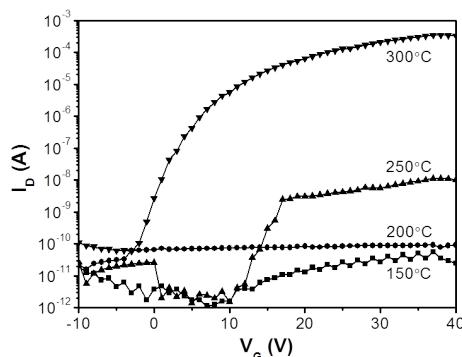


Figure 2-S. Transfer curves ( $I_D$  vs  $V_G$ ) at constant  $V_D$  of 40 V for devices annealed in air during 60 minutes at different temperatures (150, 200, 250 and 300°C).

Figure 2-S, shows the  $I_D$  vs  $V_G$  curves obtained from TFTs annealed at different temperatures and tested in air and under dark conditions at room temperature. The devices annealed at temperatures below 250°C, did not show any transistor behavior and the  $I_D$  currents were lower than  $1 \times 10^{-10}$  A. This indicates that for temperatures  $< 300^\circ\text{C}$  the films are too resistive and that films must be annealed at least at 300°C. The lowest temperature at which the devices seem to have transistor behavior (250°C) it is directly related with the decomposition temperature of cyanamide in air.<sup>5</sup> On the other hand, the sintering phenomena in which the union necks are formed between the grains,<sup>6</sup> occurs around 300°C.

SEM images corresponding to CdS annealed films at different temperatures are shown in the Figure 3-S. The films annealed at temperatures lower than 300°C exhibit granular morphologies without evident morphological changes. Furthermore, the morphology is very similar to non-annealed or annealed in nitrogen films (see Figure 6 a and b in the paper and Figure 1-Sb in the supporting information). The sintering effect however, is evident only in the films annealed in air at 300 °C, consistent with the films showing better TFT performance.

The use of higher annealing temperatures might be disadvantageous for several reasons. First, the processing cost will increase; second, it could limit the application of this technology to flexible devices. Kim *et.al.*,<sup>4</sup> found that annealing process at temperatures of 400°C and higher, the resistivity of CdS films increases despite the grain size increment. The authors attributed this effect to the decrement of cadmium excess and therefore the sulfur vacancies decreased after the annealing process.

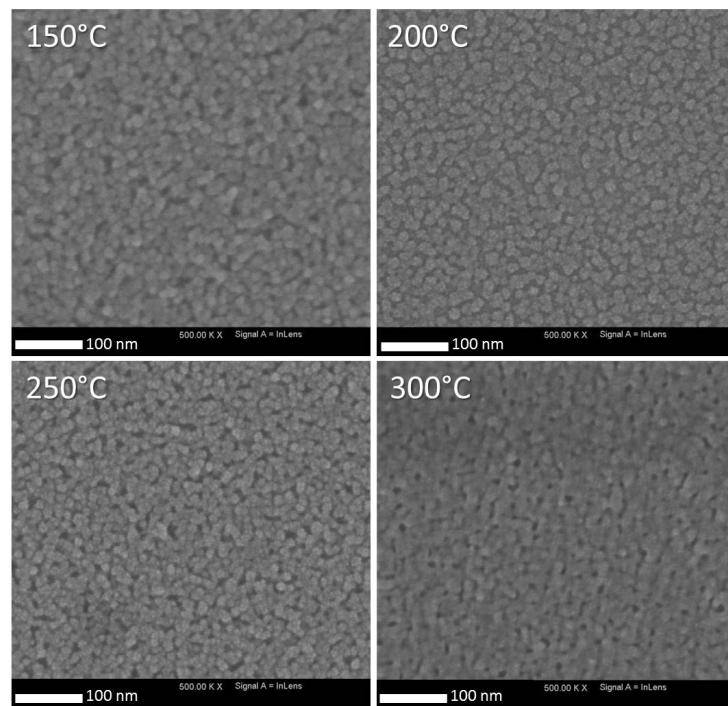


Fig. 3-S. SEM results for CdS films annealed in air during 60 minutes at different temperatures (150, 200, 250 and 300°C)

<sup>1</sup> R.I. Dimitrov, N. Moldovanska and I.K. Bonev, *Thermochimica Acta*, 2002, **385**, 41-49.

<sup>2</sup> U. Dittmar, B.J. Hendan, U. Florke and H.C. Marsmann, *J. Organomet. Chem.*, 1995, **489**, 185-194.

<sup>3</sup> A.J. Haider, A.M. Mousa and S.M. Al-Jawad. *Journal of Semiconductor Technology and Science*, 2008, **8**, 326-332.

<sup>4</sup> N. Kim, S. Ryu, H. Noh and W. Lee. *Materials Science in Semiconductor Precessing*. 2012, **15**, 125-130.

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<sup>6</sup> L.H. Liang, C.M. Shen, S. Du, W.M. Liu, X.C. Xie and H.J. Gao, *Phys. Rev B.*, 2004, **70**, 205419-205424.