Electronic Supplementary Information

Direct imprint of MoS_2 flakes on the patterned gate for nanosheet transistors†

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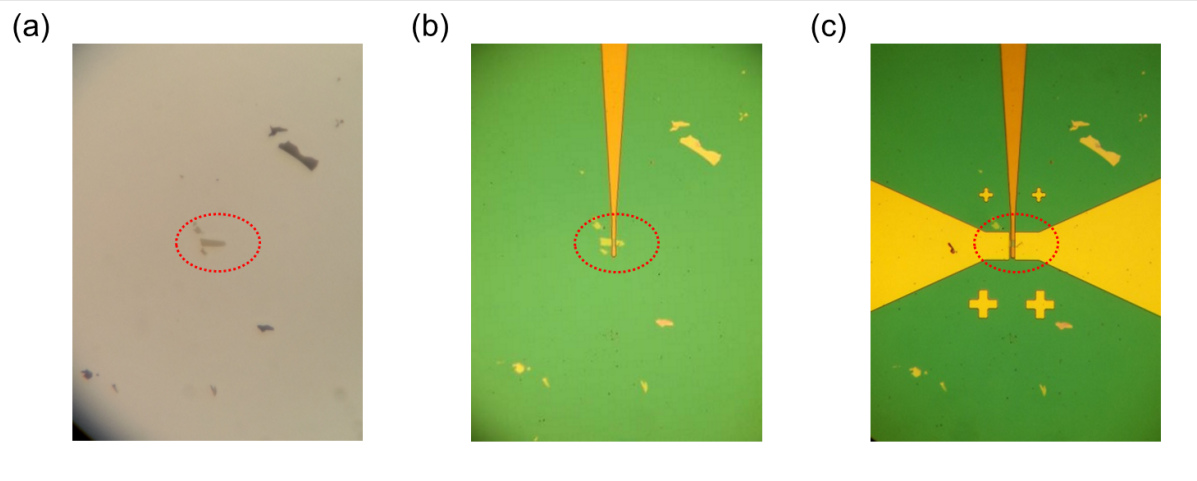

Fig. S1 Optical microscopy images of (a) an exfoliated few layer-thin MoS_2 attached on PDMS, (b) precisely imprinted MoS_2 on patterned Au gate electrode, and (c) a bottom-gate MoS_2 FET with S/D pattern of Au/Ti. Note that we use an identical MoS_2 flake for all process steps.

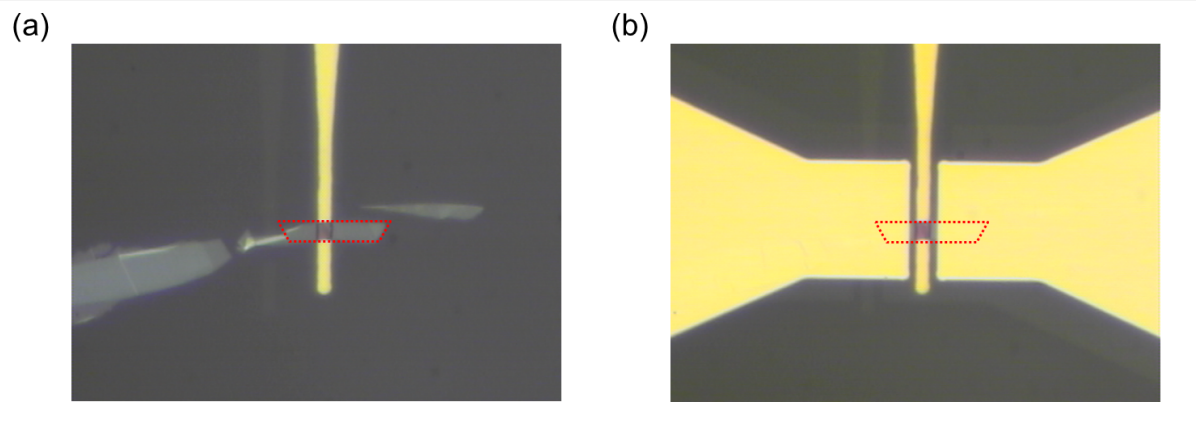

Fig. S2 Optical microscopy images of Tr3 device on glass, which has non-gated region in its FET channel: (a) before and (b) after S/D contact.