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Electronic Supplementary Information:

Selective n-Type Doping in Graphene via the Aluminium Nanoparticle Decoration Approach

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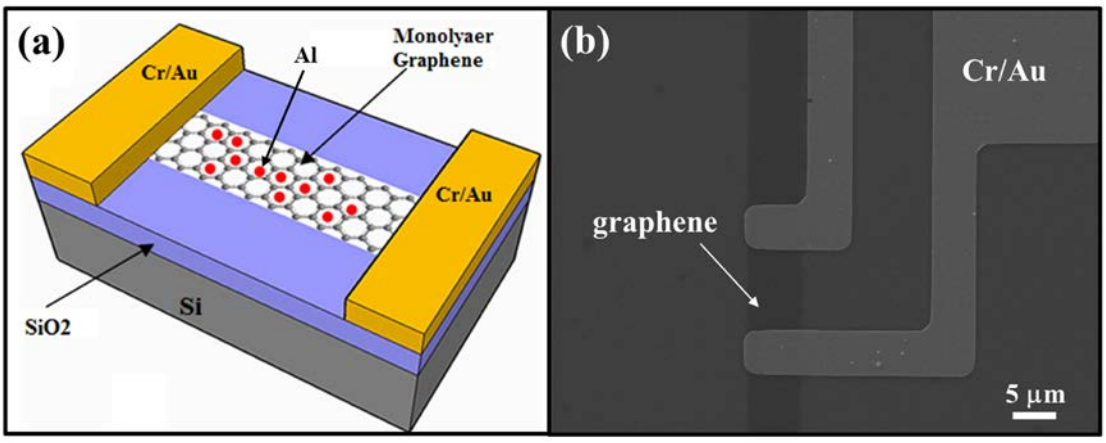

Figure S1. (a) Schematic illustration and (b) SEM image of Al decorated graphene FET.

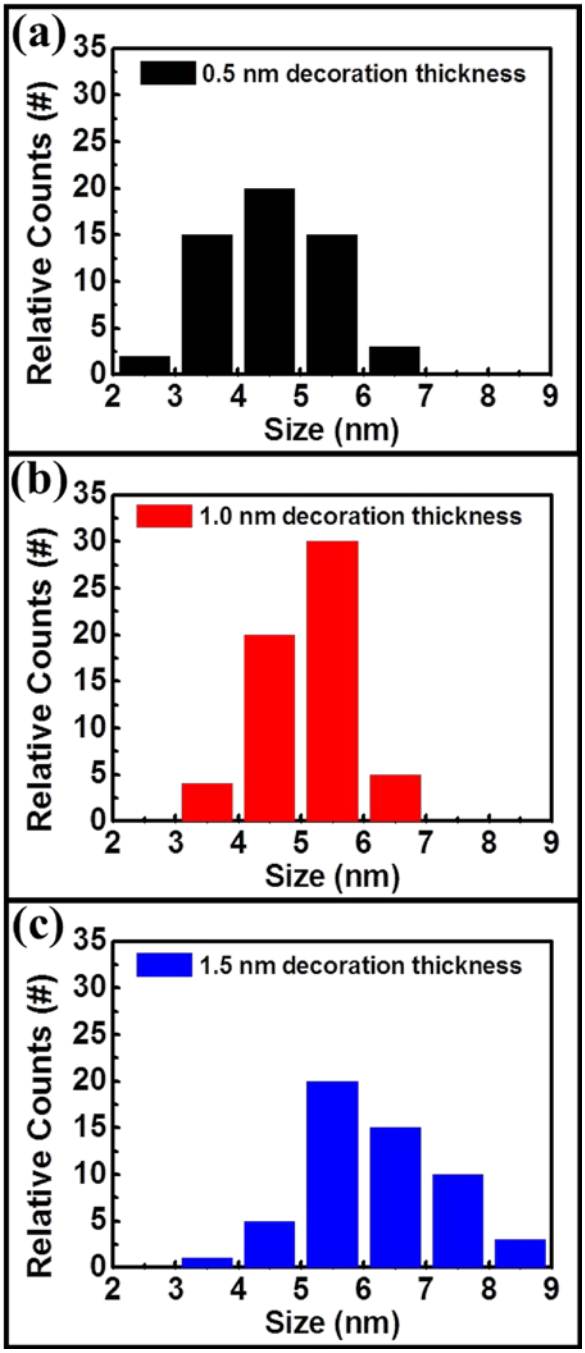

Figure S2. Size distribution of discrete Al nanoparticles deposited with different decoration thickness: (a) 0.5 nm, (b) 1.0 nm and (c) 1.5 nm.

Calculation of charge carrier density:

- The charge carrier density of graphene FETs can be calculated by the formula:

$$n = \frac{CV_D}{eS} = \frac{\varepsilon_0 \varepsilon_r V_D}{eD}$$

where C is the capacitance of the gate in the FET, V_D is the shift of the Dirac point relative to that of the pristine graphene, S is the surface area, e is the electron charge, ε_0 is the value of the absolute dielectric permittivity of classical vacuum，ε_r is the dielectric constant of SiO_2, and D is the SiO_2 layer thickness.

- For devices without the Al decoration, the Dirac point is located at a value larger than 40 V at the positive side (Figure 3b and d), corresponding to the hole concentration of ~2.84×10^{12} cm^{-2}. After the Al decoration and Al_2O_3 passivation, the hole concentration is decreased to ~1.78×10^{12} cm^{-2} (Dirac point at ~20 V; Figure 3a) and ~0.87×10^{12} cm^{-2} (Dirac point at ~10 V; Figure 3c) for devices with the 3 μm and 5 μm channel width, respectively. Importantly, the n-type conduction is evidently observed in the transfer curves (Figure 3), indicating the n-doping effect here in reducing the hole concentration.

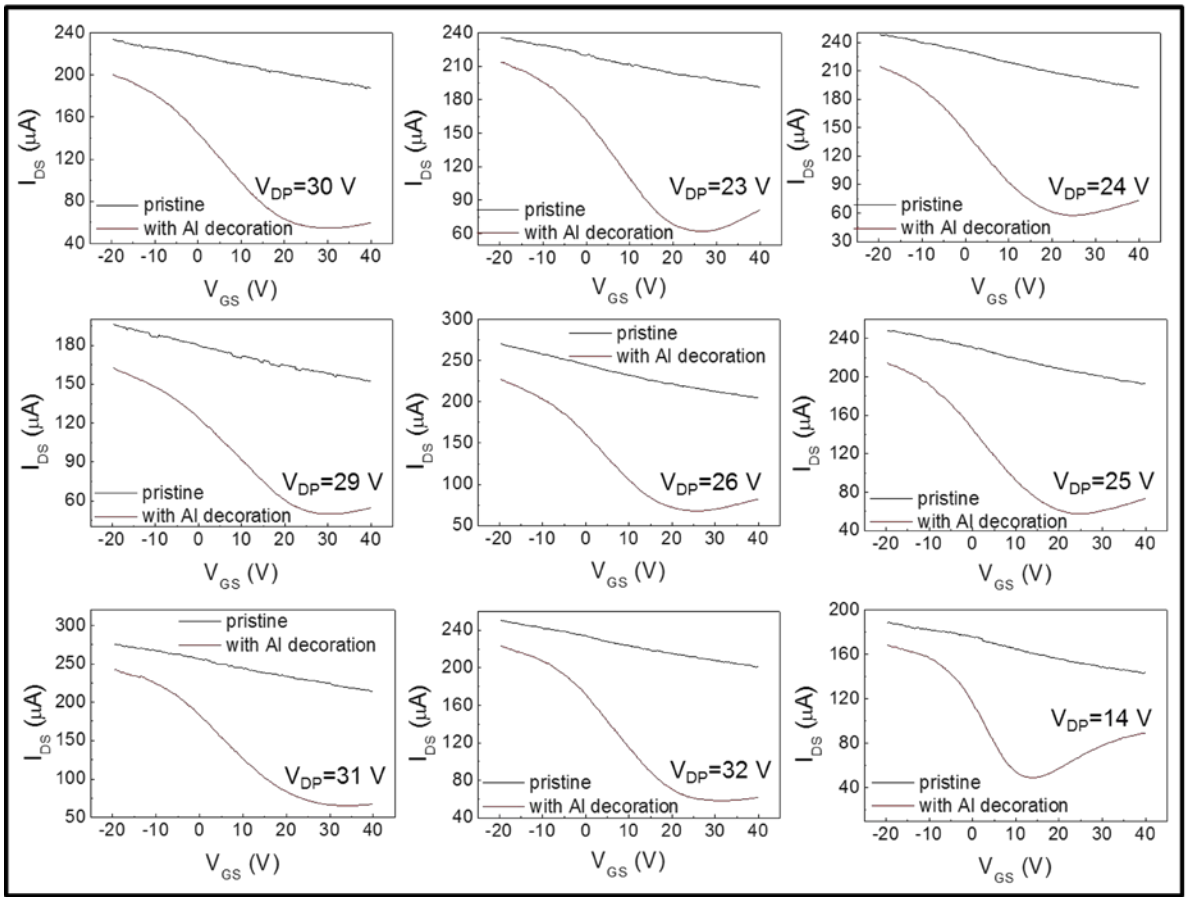

Figure S3. Transfer characteristics of nine different Al (1.0 nm thick) decorated graphene FETs. All devices are fabricated with the 3 μm channel width and the 30 nm thick Al_2O_3 capping layer. After the decoration, the Dirac point is shifted to ~26 ± 5 V for these devices.

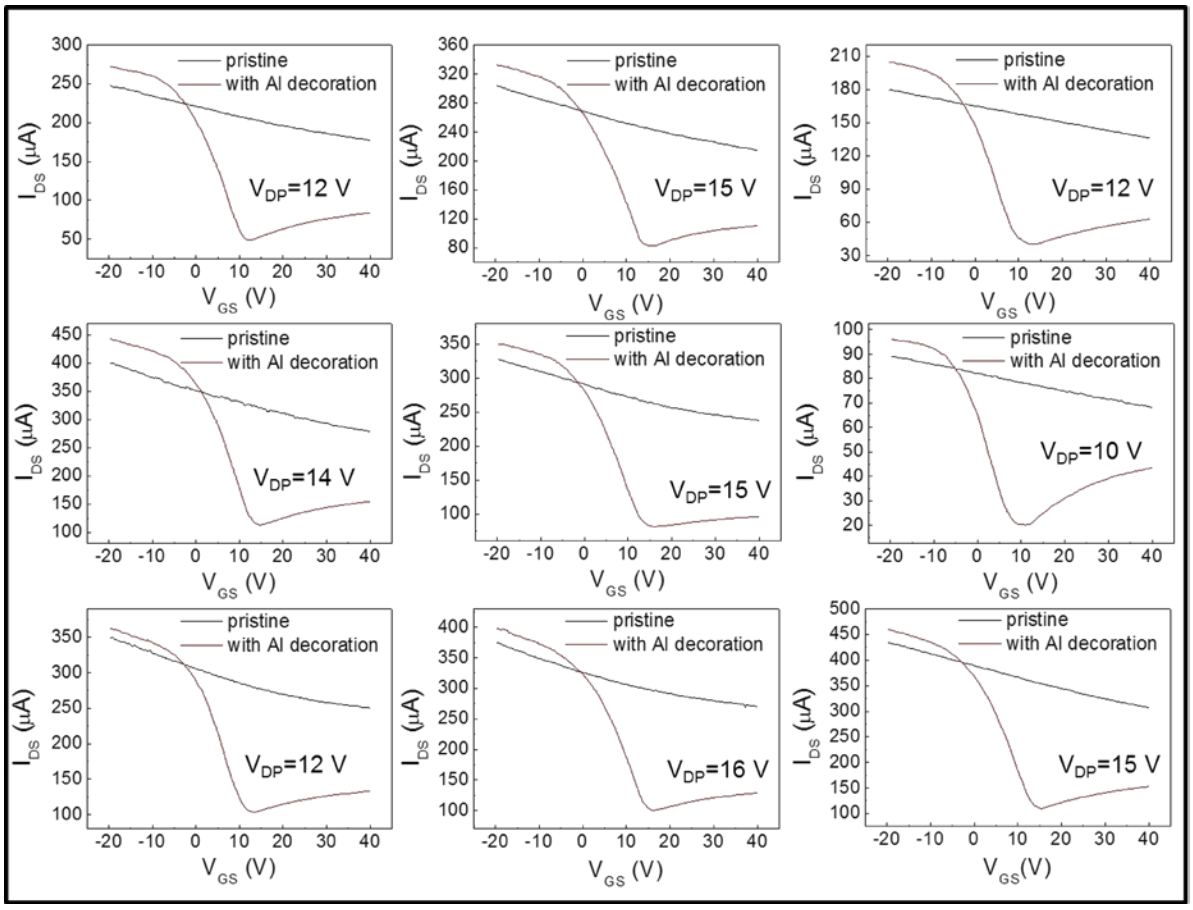

Figure S4. Transfer characteristics of nine different Al (1.0 nm thick) decorated graphene FETs. All devices are fabricated with the 5 μm channel width and the 30 nm thick Al_2O_3 capping layer. After the decoration, the Dirac point is shifted to ~13 ± 2 V for these devices.

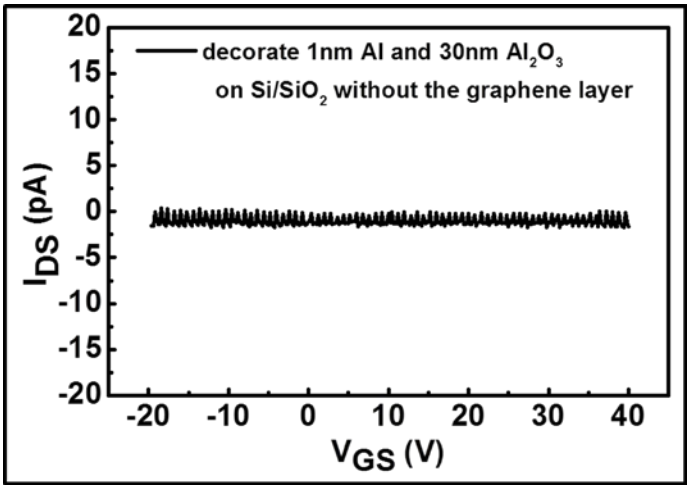

Figure S5. Transfer characteristic of the control device with only 1 nm thick Al and 30 nm Al_2O_3 passivation layer (without the active graphene channel layer).

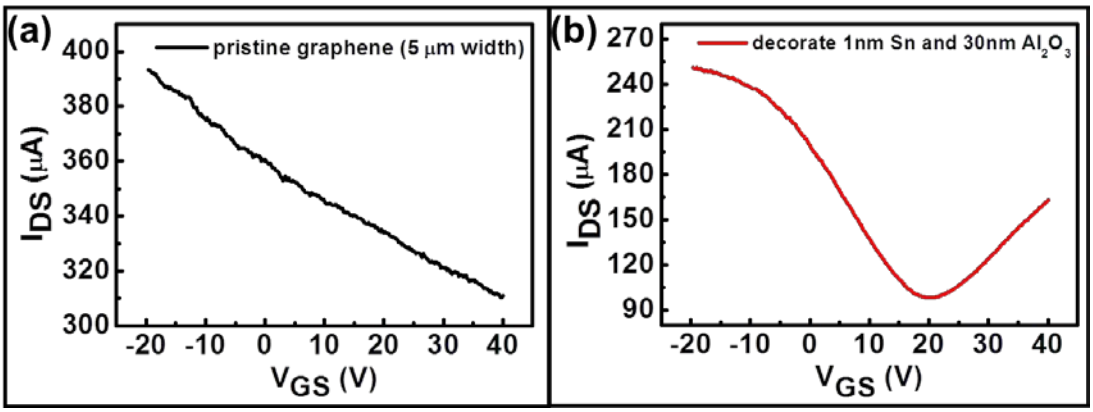

Figure S6. Transfer characteristic of the typical Sn decorated graphene FET. The Dirac point of the graphene device is shifted to +20 V with the Sn decoration.