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Electronic Supplementary Information

MoS_2 Nanosheet Channel and Guanine DNA-base Charge Injection Layer for High Performance Memory Transistors

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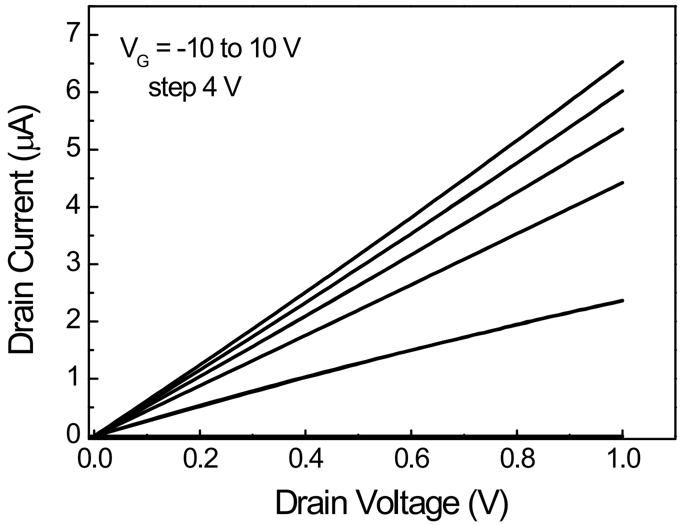

Figure S1. Output characteristics of our MoS_2 nanosheet FET (Device 1) that evidences good ohmic behavior with Ti/Au contact electrodes.

In addition, the ohmic behavior is dependent on the contact area (related to W or W/L ratio in FETs), since the larger contact area would provide smaller contact resistance for source/drain (S/D). This means that larger W or W/L ratio would provide higher I_D current eventually promoting the linear field effect mobility. In the present study, Device 1 with thinner MoS_2 and larger W/L shows much higher linear mobility of 35.7 cm^2/Vs, while Device 2 shows only 3.1 cm^2/Vs. (Device 1: 7 layer, W/L=0.95/2.6, versus Device 2: 11 layer, W/L=0.6/3).

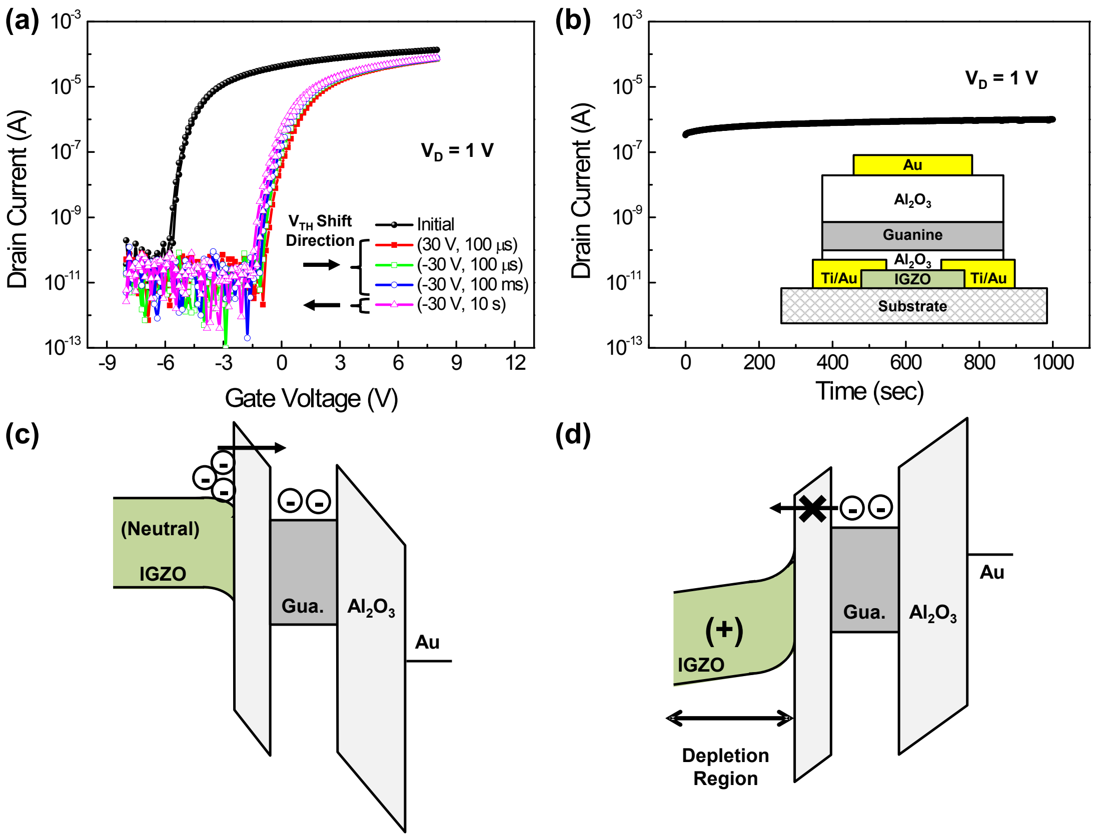

Figure S2. (a) Transfer characteristics of amorphous InGaZnO (a-IGZO) FET with guanine charge trapping layer. It seems that trapping (Program) was very possible but detrapping (Erase) is never possible. (b) Static current retention of a-IGZO memory FET after Program (trapping into guanine). Schematic device cross section is shown as the inset image. Schematic band diagrams of a-IGZO memory FET under (c) Program and (d) Erase conditions.

Comparing MoS_2 nanosheet channel to our previous study with amorphous InGaZnO (a-IGZO) thin film channel, we observe a remarkable thing. The charge ejection from guanine to MoS_2 can be carried out with only -15 V gate pulse while the a-IGZO does not show any ejection even with pulse width up to 10 s. In general, the unipolar thin film based charge trapping memory does not show the reversible program and erase characteristics. The main reason is thought to be that the erasing pulse (opposite sign to programming pulse) would make the semiconducting layer be electrically depleted, so that an effective voltage applied at dielectric would be reduced due to voltage dividing between dielectric and depleted semiconductor (the band diagram of a-IGZO is described in Figure S2(d)). In MoS_2 nanosheet case, however, the voltage drop at MoS_2 layer could be ignorable due to its extremely thin thickness.

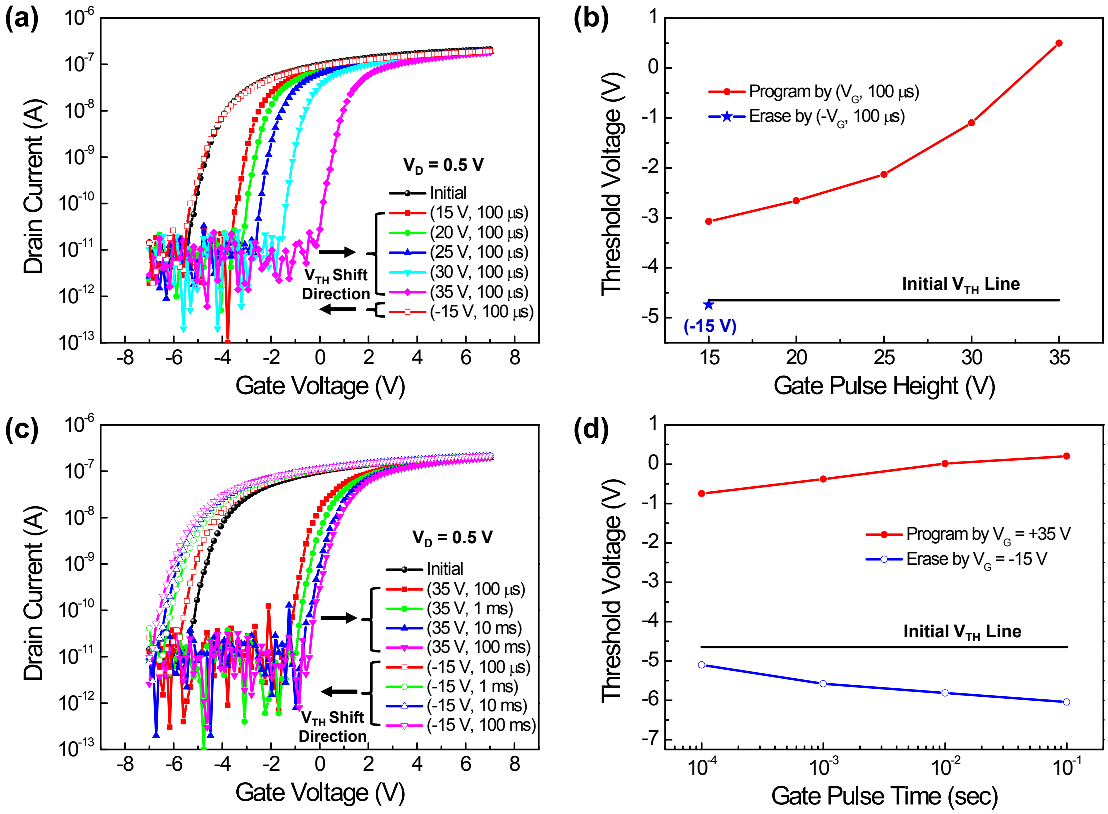

Figure S3. (a) Transfer characteristics of the Device 2 under the various gate voltage pulse height: V_G = 0 (initial), 15, 20, 25, 30, 35, and -15 V (after 35 V) under a constant pulse width (100 µs). (b) Gate pulse height versus V_{TH} plot with the same V_{TH} definition (I_D current reaches to 1 nA). (c) Transfer characteristics of the Device 2 under the various gate voltage pulse time: 100 µs, 1 ms, 10 ms, 100 ms under constant pulse height of 35 V (Program)/-15 V (Erase). (b) Gate pulse time versus V_{TH} plot. Device 2 has shown almost the same behavior as that of Device 1 in respects of memory window and V_G pulse height for memory except their mobility and transfer curve shape differences.

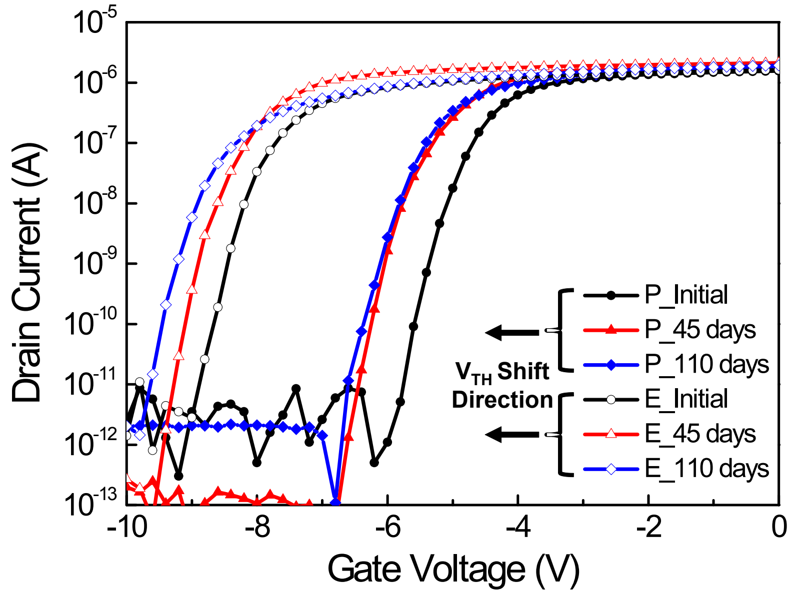

Figure S4. Program and Erase curves as memory window shift toward negative side as the da y passes, but the shifted voltages are relatively small; only 0.7 V shift is observed after 110 d ays. These effects obviously indicate the benefit of guanine layer, which could be exploited a s an aging-protection agent for nonvolatile memory.