Electronic Supplementary Information

Low-temperature annealed PbS quantum dot films for scalable and flexible ambipolar thin-film-transistors and circuits

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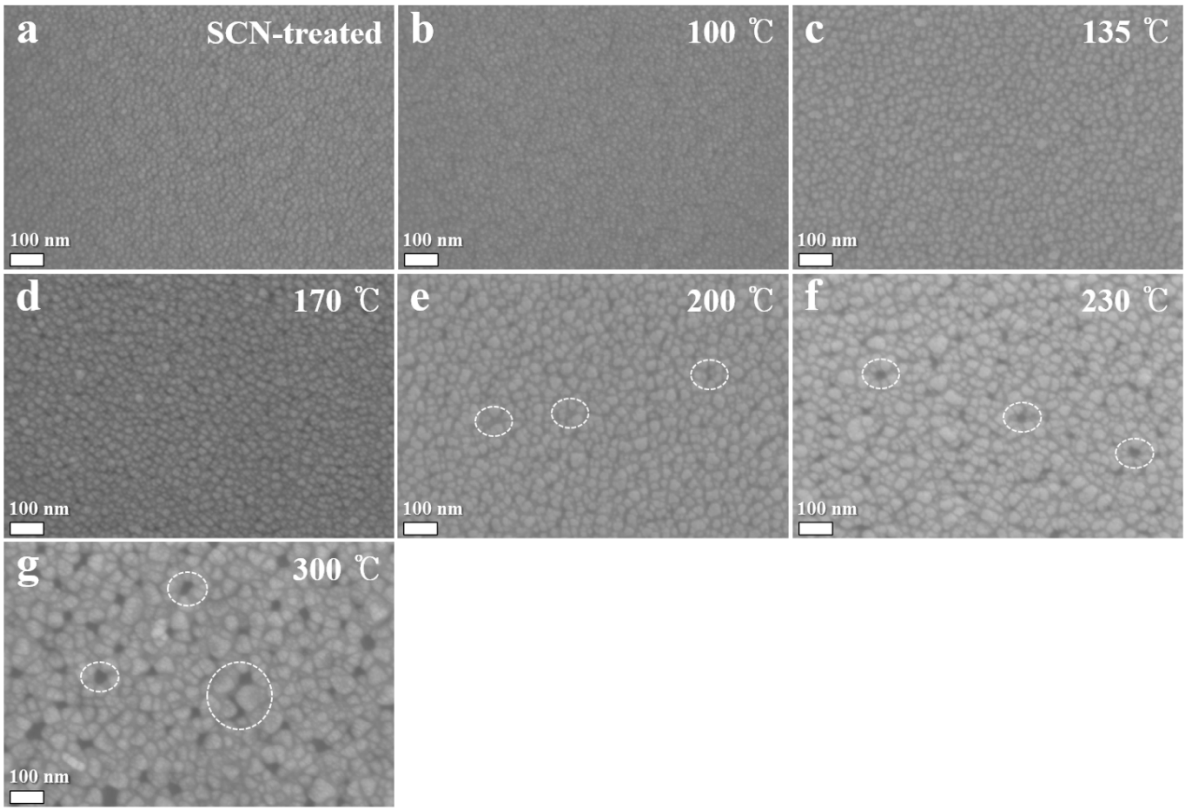

Figure S1. The field-emission scanning electron microscope images of (a) SCN-treated and then (b-g) thermally annealed PbS QD films. The white dotted circles in the pictures indicate examples of the voids (or disconnection) caused by aggregation (sintering) of QDs due to high temperature annealing. Above 200 °C, the number and the size of voids gradually increased with increasing T_a.

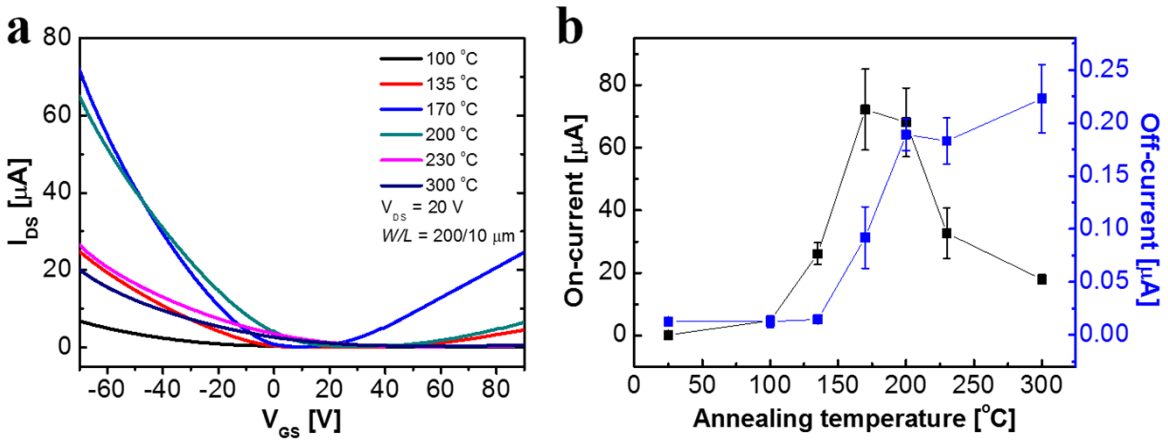

Figure S2. (a) Temperature-dependent linear scale of I_{DS}-V_{GS} transfer characteristics up to 300 °C and (b) temperature-dependent p-type on-/off- currents of SCN- and thermal-treated PbS QD TFTs with Au S/D electrodes (at V_{DS} = 20 V). The error bars indicate the standard deviation of ten devices for the p-type on-/off- currents.

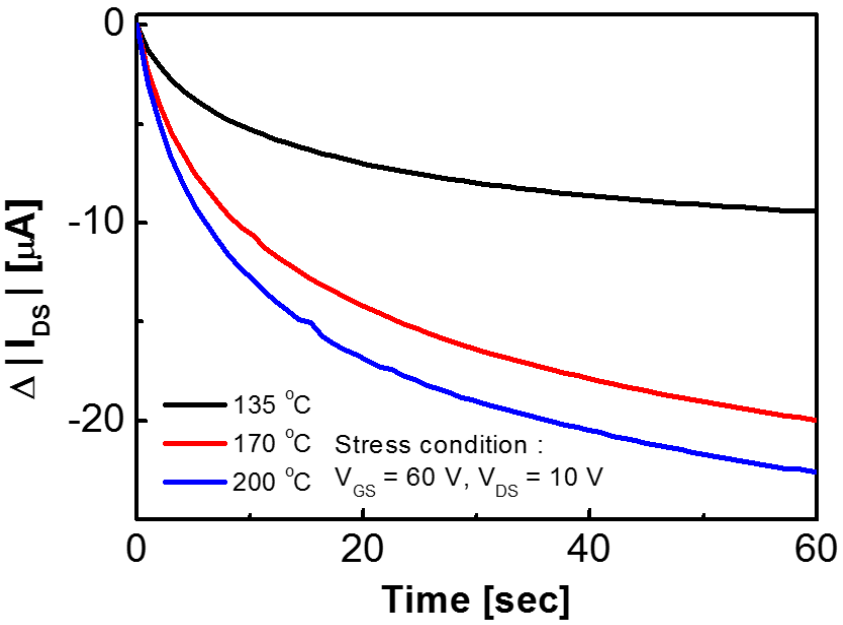

Figure S3. The variation of I_{DS} of SCN- and thermal-treated PbS QD TFTs with continuous bias stress (V_{GS} = 60 V and V_{DS} = 10 V).

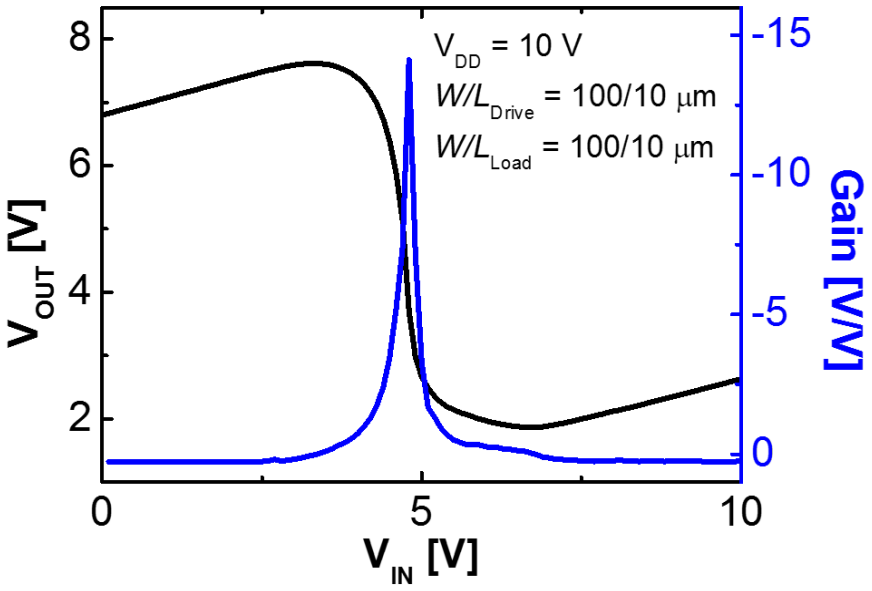

Figure S4. The transfer and gain characteristics of a CMOS inverter operating at V_{DD} of +10 V using SCN-treated and 170 °C-annealed PbS QD TFTs on ultra-thin PI. A β-ratio is 1 with $(W/L)_{\text{Load, Drive}}$ of 100 μm /10 μm and a gain of this device is approximately 14.1 V/V.

Table S1. The Scherrer equation-based grain size analysis from GIAXRD peak at 2θ = 30.1° in Figure 3c.

	SCN-treated	100 ˚C	135 ˚C	170 ˚C	200 ˚C	230 ˚C	300 ˚C
grain size [nm]	5.7	6.4	8.6	11	13.1	14	17.2