

SUPPLEMENTARY INFORMATION
for
**Mixed Self-Assembled Monolayer Gate Dielectrics For Low-Voltage Solution-
Processed Polymer Field-Effect Transistors**

Thales V.A.G. de Oliveira and Aitziber E. Lopez
CIC nanoGUNE, 20018 Donostia-San Sebastian, Basque Country, Spain

Luis E. Hueso and Alexander M. Bittner*
*CIC nanoGUNE, 20018 Donostia-San Sebastian, Basque Country, Spain and
IKERBASQUE - Basque Foundation for Science, 48011 Bilbao, Basque Country, Spain*

**to whom correspondence should be addressed: a.bittner@nanogune.eu*

Materials: Degenerately doped (As, n++) silicon wafers (500 μ m thick) with 150nm of thermally grown insulating SiO₂ were provided by Silicon Valley microelectronics Inc. and were used as substrates for all devices. Substrates had r.m.s. roughness 0.15-0.17nm. Aluminum (99.999%), Titanium (99.995%) were purchased from Kurt J. Lesker. Gold (99.999%) was purchased from Alfa Aesar. Positive tone resist PMMA 950K-A2/495K-A4, and LOR05B were purchased from MicroChem Corp. LOR05B was diluted with its appropriate thinner (PMGI Thinner T, MicroChem Corp), in order to give ca. 85nm thick films upon spin-coating at 4k rpm. Octadecylphosphonic acid (ODPA, 97%), 16-hexadecanoic acid (PHDA, 97%), 2-propanol (>99.8%), 1,2-dichlorobenzene (99%, anhydrous), and acetone (>99.5%) were purchased from Sigma-Aldrich and used as received.

Methods: Current–voltage (I–V) and capacitance–frequency (C–f) were recorded with a Keithley 4200-SCS parameter analyzer. Samples were analyzed under vacuum (<3x10⁻⁴mbar) in Lake Shore probe station after a short exposure to air (<30s). Atomic force microscopy images were taken with an Agilent Technologies 5500 system, equipped with Nanosensors PPP-NCHR AFM tips. Contact-angle measurements were performed with a G10 Krüss system. Smooth Al films were grown in a Kurt J. Lesker PVD75 system by

thermal evaporation equipped with a heat shielded tantalum crucible heater (EVCH12) and a tall intermetallic crucible liner (EVC5INTSPL03). High evaporation rates were obtained by approaching the sample to the Al source, instead of increasing the heating power. This allowed very high deposition rates, and also to avoid overheating the sample surface.

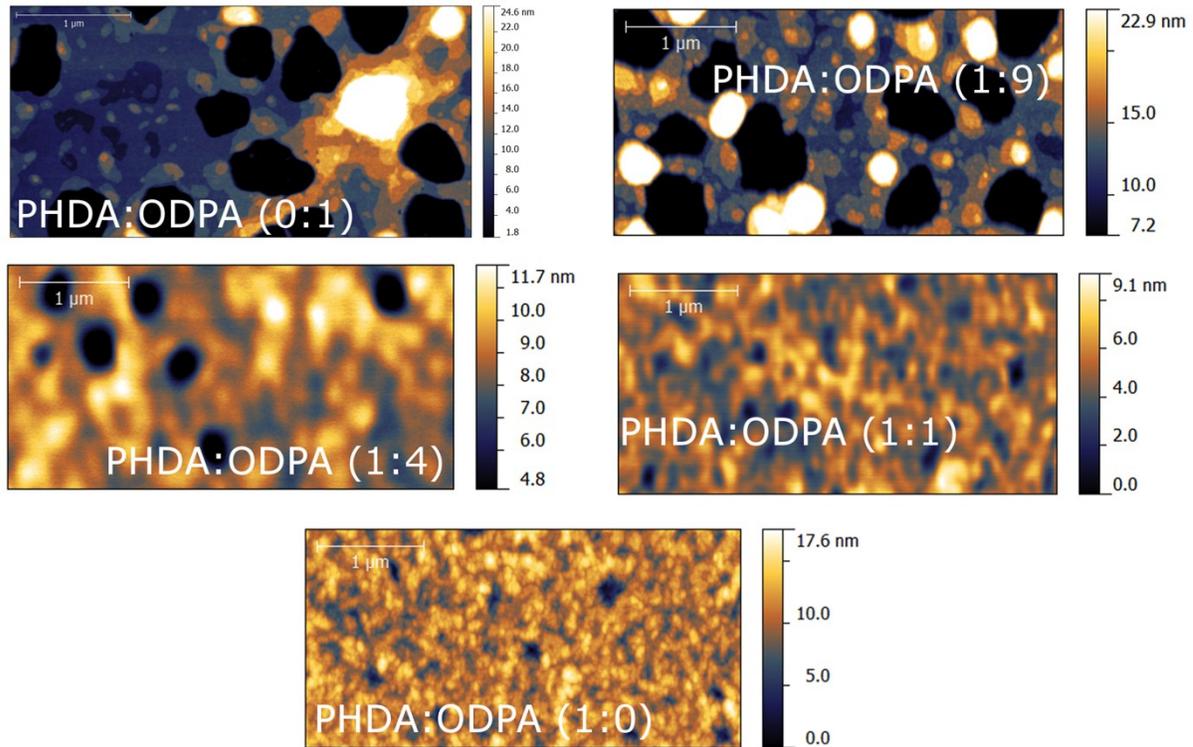


Figure S1. AFM images of spin-coated and annealed (180°C, 10min) pBTTT thin-films on ultrasmooth ODPA-healed PA-SAM/ALD-AlO_x (R_q<0.17-0.22nm). The SAM's PHDA:ODPA molar fraction was varied from (0:1, pure ODPA) to (1:0, pure PHDA). Molecular terracing is observed for the sample with the lowest fraction of PHDA (1:9), and pure ODPA (0:1). Strong dewetting is observed with these substrates. We do not observe intense dewetting with the transistors since the surface energy of exposed SiO₂ is sufficiently high for spin-coating after ODPA assembly. Dewetting is reduced as PHDA concentration is increased and, concurrently, molecular terracing is disrupted. All images were carefully taken with the same AFM tip. Sample processing and characterization was done on the same series of samples used for SCA and J-V analysis (Figure 02, main text). The tip condition was checked before and after each image with PHDA:ODPA(0:1) as reference sample. Roughness over monolayer surface measured after annealing remained unaltered, confirming the thermal stability of the PA-SAMs.

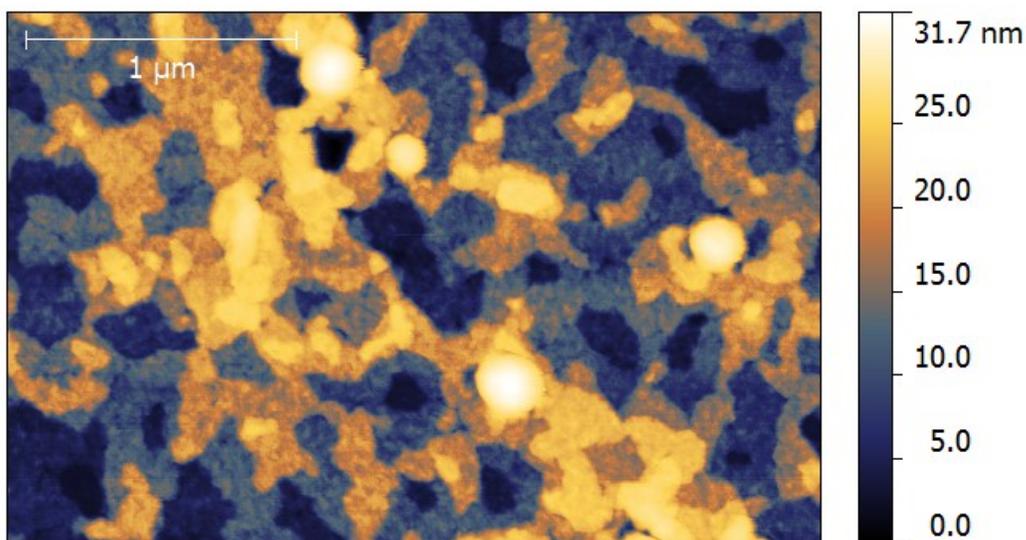


Figure S2. pBTTT thin-film on a Al(20nm)/AlOx(4nm)/ODPA gate electrode. This image represents the annealed (10min at 165°C) sample of Figure 03(a) further annealed at the same temperature for 20min. The surface roughness over the pBTTT terraces decreases only slightly with the extra annealing time.

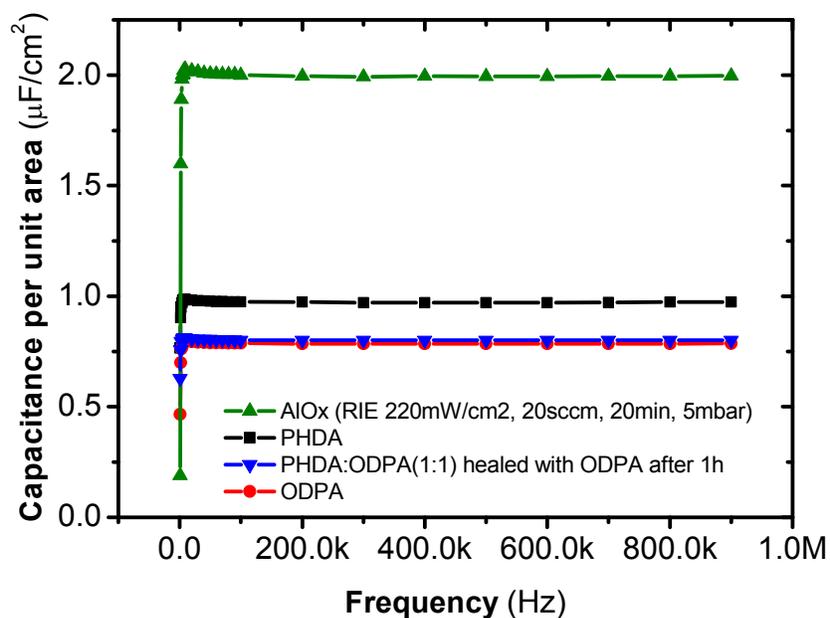


Figure S3. Capacitances of AlOx and the PA-SAM/AlOx dielectrics. The measurements were recorded with a Keithley 4200-SCS parameter analyzer, for a range of junction areas ($1.2\text{-}2.5 \times 10^{-4} \text{cm}^2$), and Au top electrodes deposited through shadow mask. The AlOx had a thickness of $\sim 4 \text{nm}$ (measured by X-Ray Reflectivity), resulting in a calculated relative permittivity of $\epsilon \approx 9$. The increased areal capacitance of the PHDA-only

layer can be attributed to a higher defect density of the SAM. The measurement was done with DC bias 3V, and AC bias 30mV with frequencies up to 1 MHz.

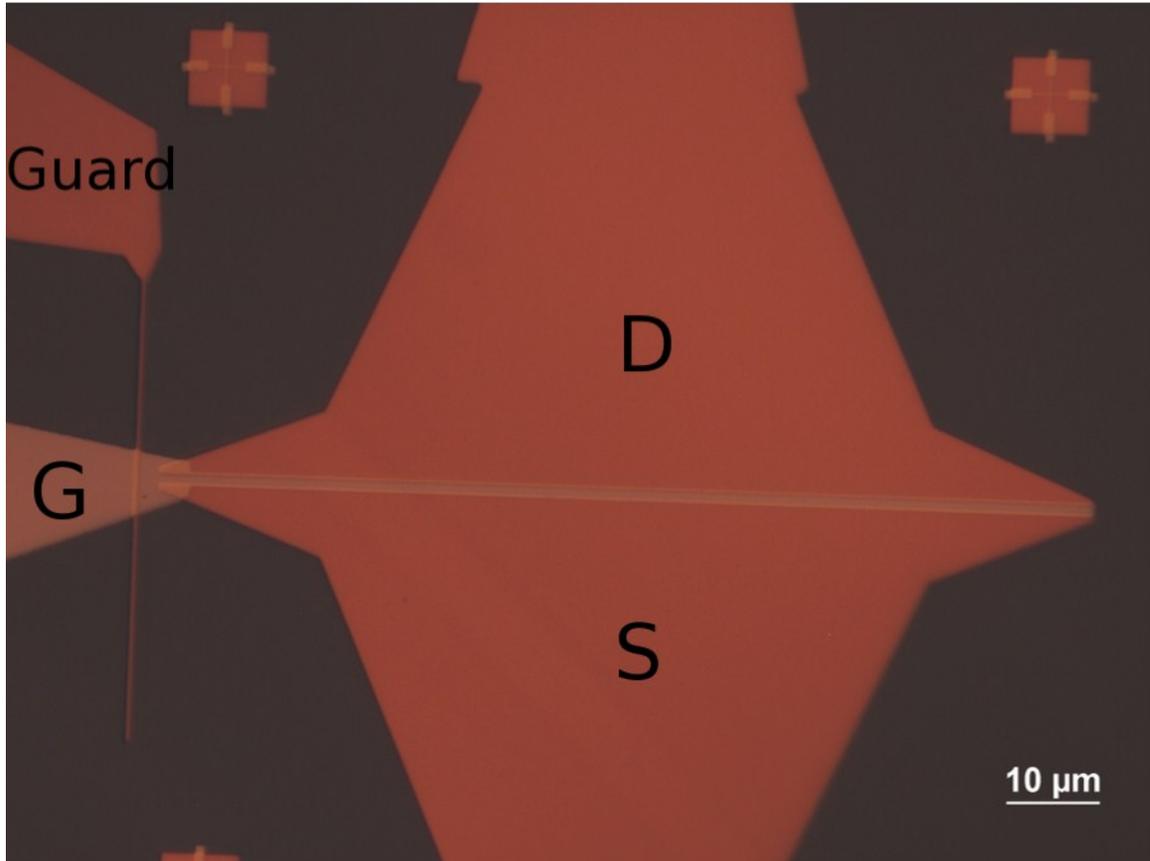


Figure S4. Optical microscopy image of a typical transistor. Source (Au), drain (Au), guard (Au), and gate (Al/AlO_x/PA-SAM) electrodes are clearly visible in the image. Channel length (L) is 1μm, whereas the width (W) is 100μm. pBTTT thin-films are spin-coated onto these structures in order to complete the fabrication process.